# Kolhapur Institute of Technology's College of Engineering (AUTONOMOUS), Kolhapur.

(An Autonomous Institute)



# Syllabus

# S.Y. B. Tech.

# **Computer Science & Engineering**



| Title of the Course: Computational Mathematics                                    | L      | Т       | Р      | Credits   |  |  |  |  |
|---|--------|---------|--------|-----------|--|--|--|--|
| Course Code: UCSE301  | 3      | 1       |        | 4         |  |  |  |  |
| Course Pre-Requisite: Basics of Matrix Algebra, Rules and Formulae of Derivative, |        |         |        |           |  |  |  |  |
| Basic Statistical Concepts, Set Theory.   |        |         |        |           |  |  |  |  |
| Course Description: This Course contains Advanced Linear Algebra, Numerical       |        |         |        |           |  |  |  |  |
| Methods, Probability Distributions, Statistical Techniques and Fuzzy Sets.        |        |         |        |           |  |  |  |  |
| Course Objectives:  |        |         |        |           |  |  |  |  |
| 1. To learn mathematical methodologies and models since ma                        | themat | tics is | the fo | oundation |  |  |  |  |
| of engineering and technology.  |        |         |        |           |  |  |  |  |
| 2. To develop mathematical skills and enhance logical thinkin                     | g pow  | er of s | studer | nts.      |  |  |  |  |

- To provide students with skills in advanced linear algebra, probability, statistical techniques and fuzzy sets which would enable them to devise engineering solutions for given situations they may encounter in their profession.
- 4. To increase interest towards the use of mathematics in engineering module.

#### **Course Outcomes:**

| COs | After the completion of the course the student will be able to                                   |
|-----|--|
| CO1 | <b>Find</b> numerical solution of algebraic and transcendental equations using numerical method. |
| CO2 | <b>Explain</b> the fuzzy sets and fuzzy logic in dealing with real problems.                     |
| CO3 | Make use of method of least squares to fit the curves for given bivariate data.                  |
| CO4 | Apply the knowledge of probability distributions to solve problems arising in engineering.       |
| CO5 | <b>Solve</b> the systems of simultaneous linear equations using factorization method.            |
| CO6 | <b>Determine</b> fuzzy numbers and <b>use</b> it in fuzzy equations.                             |

#### **CO-PO Mapping:**

|            |    | -  |    | -  |    |    |    | -          |    | -  | -  |    |    | -  |
|------------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|
| CO         | PO | <b>PO8</b> | PO | PO | PO | PO | PS | PS |
|            | 1  | 2  | 3  | 4  | 5  | 6  | 7  |            | 9  | 10 | 11 | 12 | 01 | 02 |
| CO1        |    | 2  |    |    |    |    |    |            |    |    |    |    |    |    |
| CO2        | 3  |    |    |    |    |    |    |            |    |    |    |    |    |    |
| CO3        |    |    | 3  |    |    |    |    |            |    |    |    |    |    |    |
| CO4        |    | 3  |    |    |    |    |    |            |    |    |    |    |    | 1  |
| <b>CO5</b> |    |    |    | 2  |    |    |    |            |    |    |    |    |    | 1  |
| <b>CO6</b> |    |    | 2  |    |    |    |    |            |    |    |    |    |    |    |

#### Assessments :

#### **Teacher Assessment:**

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weights respectively.

| Assessment | Marks |
|------------|-------|
| ISE 1      | 10    |

| MSE  | 30                                       |                  |  |  |  |  |
|--|--|------------------|--|--|--|--|
| ISE 2  | 10                                       |                  |  |  |  |  |
| ISE 1 and ISE 2 are based on assignment/decl   | ared test/quiz/seminar/Group Discussions | etc.             |  |  |  |  |
| MSE: Assessment is based on 50% of course of ESE: Assessment is based on 100% of course of | content (Normally first three units)     |                  |  |  |  |  |
| (normally last three units) covered after MSE  |  |                  |  |  |  |  |
| Course Contents:   |  |                  |  |  |  |  |
| Unit 1: Advanced Linear algebra  |  | 7<br><b>Hrs.</b> |  |  |  |  |
| 1. Revision of linear dependence of ve   | ctors.                                   |                  |  |  |  |  |
| 2. Solutions of simultaneous linear equ  | ations using Gauss-Jordan method.        |                  |  |  |  |  |
| 3. Solutions of simultaneous linear equ  | nations using LU decomposition method.   |                  |  |  |  |  |
| 4. Determination of Eigen Value by Ite   | eration method.                          |                  |  |  |  |  |
| 5. Solution of non-linear simultaneous   | equations.                               |                  |  |  |  |  |
| Unit 2: Numerical methods  |  | 6<br>Hrs         |  |  |  |  |
| 1. Solutions of algebraic and transcend  | lental equations methods.                | 111 5.           |  |  |  |  |
| 2. Bisection method.   |  |                  |  |  |  |  |
| 3. Newton-Raphson method.  |  |                  |  |  |  |  |
| 4. Secant method.  |  |                  |  |  |  |  |
| 5. Numerical Integration.  |  |                  |  |  |  |  |
| 6. Simpsons 1/3 and 3/8 rules.   |  |                  |  |  |  |  |
| 7. Weddle's rule.  |  |                  |  |  |  |  |
| Unit 3: Probability and Distribution   | S  | 8<br>Hrs         |  |  |  |  |
| 1. Introduction of probability.  |  |                  |  |  |  |  |
| 2. Laws of probability.  |  |                  |  |  |  |  |
| 3. Conditional probability.  |  |                  |  |  |  |  |
| 4. Baye's Theorem.   |  |                  |  |  |  |  |
| 5. Random variables.   |  |                  |  |  |  |  |
| 6. Discrete distributions: Binomial and  | Poisson.                                 |                  |  |  |  |  |
| 7. Continuous distributions: Normal.   |  |                  |  |  |  |  |

| Unit 4: Statistical Techniques   | 8                |
|--|------------------|
| 1. Lines of regression of bivariate data, Correlation coefficient.   | Hrs.             |
| 2. Fitting of Curves by method of Least-squares.   |                  |
| 3. Fitting of Straight lines.  |                  |
| 4. Fitting of Parabola.  |                  |
| 5. Fitting of Exponential curves.  |                  |
| 6. Tests of significations: Z-test, t-test (For single mean)   |                  |
| 7. Chi-square test for independences of Attributes.  |                  |
| Unit 5: Introduction to Fuzzy sets and Fuzzy Logic   | 7<br><b>Hrs.</b> |
| 1. Crisp Sets: An overview.  |                  |
| 2. Fuzzy sets: Basic concepts  |                  |
| 3. Operations on fuzzy sets.   |                  |
| 5. Multivalued Logics.   |                  |
| 6. Inference from conditional fuzzy propositions.  |                  |
| Unit 6: Fuzzy Arithmetic   | 8<br>Hrs         |
| 1. Fuzzy numbers.  | 1115.            |
| 2. Fuzzy cardinality   |                  |
| 3. Operations on Fuzzy numbers.  |                  |
| 4. Fuzzy equations of type $A + X = B$ and $A \cdot X = B$ .   |                  |
|  |                  |
| <b>Reference Books:</b><br>1. Higher Engineering Mathematics by Dr. B. S. Grewal.                                      |                  |
| <ol> <li>Linear Algebra by Seymour Lipschutz.</li> <li>Euzzy sets and Euzzy Logic by George L Klir, Bo Yuan</li> </ol> |                  |
| <ul><li>4. Probability and Statistics for Computer science by James L. Johnon.</li></ul>                               |                  |
| 5. Fundamentals of Mathematical Statistics by Gupta and Kapoor.  |                  |
| Unit wise Measurable Learning Outcomes:  |                  |

# Unit 1:--- Advanced Linear algebra

Students are able to

a) Solve simultaneous linear and non linear equations.

b) Determine Eigen Value by Iteration method.

# Unit 2:--- Numerical methods.

Students are able to

a) Evaluate integration numerically by Simpsons formulae.

b) Solve transcendental and algebraic equations by using numerical method.

# Unit 3:--- Probability and Distributions.

Students are able to

a) Define random variable.

b) Verify the function as probability function.

c) useful to determine a reasonable distributional model for the data.

# **Unit 4:--- Statistical Techniques**

Students are able to

a) Measure the correlation between bivariate data.

b) Apply fitting of curves for bivariate data.

c) Make use of Testing of Hypothesis.

# Unit 5:--- Introduction to Fuzzy sets and Fuzzy Logic

Students are able to

a) Understand Basic concept of Fuzzy set theory.

b) Define membership functions.

c) Apply Basic operations on Fuzzy set.

# Unit 6:--- Fuzzy Arithmetic

Student are able to

a) Determine Fuzzy numbers and Fuzzy cardinality.

b) Apply operate arithmetic operations on fuzzy numbers.

c) Solve fuzzy equations.

| Title of the Course: Discrete Mathematical Structures | L | Т | Р | Credits |
|---|---|---|---|---------|
|   |   |   |   |         |

| Course Code: UCSE302  | 3 | 1 |  | 4 |  |  |  |
|---|---|---|--|---|--|--|--|
| Course Pre-Requisite: Mathematics - Probability theory, Set theory.                           |   |   |  |   |  |  |  |
| Course Description: This Course consists of concepts of Discrete mathematical structures such |   |   |  |   |  |  |  |

as Set theory, Algebraic systems, Lattices, Graphs, Counting theory etc.

#### **Course Objectives:**

- 1. To use mathematically correct terminology and notations.
- 2. To understand and critically analyze, formulate and solve the mathematical problems and proofs
- 3. To understand the concepts of Discrete Mathematics such as Sets, Algebraic Systems, Graphs, Groups and lattices
- 4. To design and implement experiments on Discrete Structures Truth tables of statement formula, Set Operations, tree traversal techniques etc

#### **Course Outcomes:**

| COs | After the completion of the course the student will be<br>able to   |  |  |  |  |  |
|-----|---|--|--|--|--|--|
| CO1 | Explain the discrete mathematical structures such as Sets, Algebraic systems,<br>Groups, Probability in the field of Computer Science |  |  |  |  |  |
| CO2 | Solve the problems related to the topics on discrete mathematics  |  |  |  |  |  |
| CO3 | Make use of discrete mathematical terminology and concepts in different areas of Computer Science.                                    |  |  |  |  |  |
| CO4 | Develop the implementation of functions and algorithms related to Discrete structures.  |  |  |  |  |  |

#### **CO-PO Mapping:**

| СО  | PO1 | PO 2 | PO<br>3 | PO<br>4 | PO<br>5 | PO<br>6 | PO<br>7 | PO<br>8 | PO<br>9 | PO<br>10 | PO<br>11 | PO<br>12 | PSO<br>01 | PSO<br>02 |
|-----|-----|------|---------|---------|---------|---------|---------|---------|---------|----------|----------|----------|-----------|-----------|
| CO1 | 3   |      | 5       |         | 5       | 0       | 1       | 0       | ,       | 10       |          | 12       | 01        | 02        |
| CO2 |     | 3    |         |         |         |         |         |         |         |          |          |          |           | 1         |
| CO3 |     | 3    |         |         |         |         |         |         |         |          |          |          | 1         |           |
| CO4 |     |      | 2       |         |         |         |         |         |         |          |          |          |           | 1         |

#### Assessments :

Teacher Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weights respectively.

| Assessment  | Marks |  |  |  |  |  |
|---|-------|--|--|--|--|--|
| ISE 1   | 10    |  |  |  |  |  |
| MSE   | 30    |  |  |  |  |  |
| ISE 2   | 10    |  |  |  |  |  |
| ESE   | 50    |  |  |  |  |  |
| ISE 1 and ISE 2 are based on assignment/declared test/quiz/seminar/Group Discussions etc. |       |  |  |  |  |  |

MSE: Assessment is based on 50% of course content (Normally first three units)

ESE: Assessment is based on 100% course content with60-70% weightage for course content (normally last three units) covered after MSE.

| Course Contents:  |              |
|---|--------------|
| Unit 1: Mathematical logic (Text book-1)  | 8 Hrs        |
| 1.1 Statements and Notations  |              |
| 1.2 Connectives - negation, Conjunction, disjunction, conditional, bi-conditional, Statement  |              |
| formulas and truth tables, well formed formulas, Tautologies, Equivalence of formulas,  |              |
| Duality law, Tautological implications, functionally complete sets of connectives, other  |              |
| connectives   |              |
| 1.3 Normal and principal normal forms, completely parenthesized infix and polish notations  |              |
| 1.4 Theory of Inference for statement calculus – validity using truth table, rules of inference,  |              |
| consistency of Premises and indirect method of proof.   |              |
| Unit 2: Set theory (Text book-1)  | 8 <b>Hrs</b> |
| 2.1 Basic concepts of set theory, Operations on sets, Ordered pairs, Cartesian Products   |              |
| 2.2 Representation of discrete structures   |              |
| 2.3 Relation and ordering - properties of binary relations in a set, Relation matrix and the graph of a relation, Partition and Covering of set, Equivalence relations, Composition of Binary relations, Partial ordering, POSET and Hasse diagram. |              |
| 2.4 Functions – types, composition of functions, Inverse functions.   |              |
| Unit 3: Algebraic systems (Text book-1)   | 5 Hrs        |
| 3.1 Algebraic systems, properties and examples  |              |
| 3.2 Semigroups and Monoids, properties and examples, Homomorphism of Semigroups and Monoids   |              |
| 3.3 Groups: Definition and examples, Subgroups and homomorphism   |              |
| Unit 4: Lattices and Boolean algebra (Text book-1)  | 5 Hrs        |
| 4.1 Lattice as POSETs, definition, examples and properties  |              |
| 4.2 Lattice as algebraic systems, Special lattices  |              |
| 4.3 Boolean algebra definition and examples   |              |
| 4.4 Boolean functions   |              |
| Unit 5: Permutations, Combinations and Probability theory (Text book-2)   | 7 Hrs        |
| 5.1 The Basics of Counting  |              |
| 5.2 The Pigeonhole Principle  |              |
| 5.3 Permutations and Combinations   |              |
| 5.4 Generalized Permutations and Combinations   |              |
| 5.5 Discrete Probability  |              |

| 5.6 Conditional probability   |                      |
|---|----------------------|
| 5.7 Bayes' Theorem  |                      |
| Unit 6: Graphs (Text book-2)  | 7 <b>Hrs.</b>        |
| 5.1 Introduction to Graphs  |                      |
| 5.2 Graph Terminology   |                      |
| 5.3 Representing Graphs and Graph Isomorphism   |                      |
| 5.4 Connectivity  |                      |
| 5.5 Euler and Hamilton Paths  |                      |
| 5.6 Planar Graphs   |                      |
| 5.7 Introduction to Trees   |                      |
| Text Books:   |                      |
| <ol> <li>Discrete Mathematical Structures with Application to Computer Science - J. P. Tremb<br/>Manohar (MGH International)</li> <li>Discrete Mathematics and its Applications - Kenneth H. Rosen (AT&amp;T Be<br/>(mhhe.com/rosen)</li> </ol> | lay & R.<br>ll Labs) |
| Reference Books:  |                      |

1. Discrete Mathematics - Semyour Lipschutz, MarcLipson (MGH), Schaum's outlines.

2. C. L. Liu and D. P. Mohapatra, "Elements of Discrete Mathematics", SiE Edition, TataMcGrawHill, 2008,ISBN 10:0-07-066913-9

3. Schaums Solved Problem Series – Lipschutz.

4. Discrete Mathematical Structures – Bernard Kolman, Robert Busby, S.C.Ross and NadeemurRehman (Pearson Education)

| Title of the Course: Data StructuresLPTCredits |  |                  |                    |                    |         |          |         |         |         | its      |          |             |             |          |
|--|--|------------------|--------------------|--------------------|---------|----------|---------|---------|---------|----------|----------|-------------|-------------|----------|
| Course C                                       | ode:   | UCSE             | 20303              |                    |         |          |         |         | 3       | 3        | -        | -           | 3           |          |
| Course P                                       | re-re  | quisit           | e: Con             | nputer             | Progra  | ammin    | g       |         |         |          |          |             |             |          |
| Course O                                       | bject  | ives:            |                    |                    |         |          |         |         |         |          |          |             |             |          |
| 1. T   | o lear   | n basio          | c conce            | epts of            | Clang   | guage.   |         |         |         |          |          |             |             |          |
| 2. T   | o bec  | ome fa           | miliar             | with a             | idvanc  | ed data  | a struc | tures s | uch as  | Stacks   | , Queue  | es, Trees o | etc.        |          |
| 3. T<br>S                                      | o ana<br>tacks,  | lyze ar<br>Trees | nd solv<br>, and C | ve prob<br>Graphs. | lems u  | ising a  | dvance  | ed data | struct  | ures su  | ch as L  | ists, Link  | ed Lists, ( | Queues,  |
| 4. T   | o wri  | te prog          | grams              | on Linl            | ked Lis | sts, Do  | ubly L  | inked   | Lists,  | Trees e  | tc.      |             |             |          |
| Course O                                       | utco   | nes:             |                    |                    |         |          |         |         |         |          |          |             |             |          |
| СО   | Afte   | er com           | pletio             | n of the           | e cours | se a stu | dent s  | hould l | be able | e to:    |          |             |             | 7        |
|  |  |                  |                    |                    |         |          |         |         |         |          |          |             |             |          |
| CO 1   | Def  | ine the          | basic              | terms              | of Lin  | ear Lis  | ts, Li  | nked L  | ist, Do | oubly L  | inked I  | List, Non   | Linear      | _        |
| 01   | Dat  | a Struc          | ctures(            | Binar              | y Trees | s, AVI   | . Trees | s, Grap | hs)     |          |          |             |             |          |
| CO 2   | Cho  | ose th           | e appr             | opriate            | and o   | ptimal   | data s  | tructu  | e for a | a specif | ied app  | lication    |             |          |
| CO 3   | Ana  | lyze T           | ïme C              | omple              | xity ar | nd Men   | nory C  | Comple  | xity o  | f differ | ent algo | orithms     |             |          |
| CO 4   | CO 4 Write programs and applications with Static and Dynamic data structures |                  |                    |                    |         |          |         |         |         |          |          |             |             |          |
| Mapping  | of co  | ourse o          | outcon             | nes wit            | h pro   | gramo    | outcor  | nes:    |         |          |          |             |             |          |
| COs  | PO<br>1  | PO<br>2          | PO<br>3            | PO<br>4            | PO<br>5 | PO<br>6  | PO<br>7 | PO<br>8 | PO<br>9 | PO<br>10 | PO<br>11 | PO12        | PSO1        | PSO2     |
| CO1  | 3  | -                | -                  | -                  | -       | -        | -       | -       | -       | -        | -        | -           | 2           | 2        |
| CO2  | 3  | -                | -                  | -                  | -       | -        | -       | -       | -       | -        | -        | -           | 2           | 2        |
| CO3  | -  | 2                | -                  | -                  | -       | -        | -       | -       | -       | -        | -        | -           | 1           | 1        |
| CO4  | -  | -                | 2                  | -                  | -       | -        | -       | -       | -       | -        | -        | -           | 3           | 3        |
| Assessme                                       | nt:  |                  |                    |                    |         |          |         |         |         |          |          |             |             | <u> </u> |

#### **Teacher Assessment:**

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weights respectively.

| Assessment | Marks |
|------------|-------|
|            |       |

| ISE-I   | 10   |           |  |  |
|---|--|-----------|--|--|
| ISE-II  | 10   |           |  |  |
| MSE   | 30   |           |  |  |
| ESE   | 50   |           |  |  |
| Course Contents:  |  |           |  |  |
| Unit 1: Basics of Data Structure:   |  | 06        |  |  |
| Abstract Data Type (ADT), control struct<br>Space and Time Complexity, Recursion,   | ure, array, function, structure, pointer, Algorithm,<br>Towers of Hanoi and Ackermann's function, etc. | Hrs       |  |  |
| Unit 2: Stacks and Queues:  |  |           |  |  |
| <ul><li>Stack: Definition, representation, implementation, applications of stack for expression evaluation and conversion</li><li>Queue: Definition, representation, implementation, applications of queue, circular queue and priority queue</li></ul> |  |           |  |  |
| Unit 3: Linked Lists:<br>Definition, representation, implementation<br>lists, stack and queue implementation using  | on and operations on singly, doubly and circular linked<br>ng linked list                              | 09<br>Hrs |  |  |
| Hashing: Hashing functions, overflow handling, open and closed hashing, rehashing   |  |           |  |  |
| Unit 4: Searching and Sorting Techniques:<br>Search: Importance of searching, types- sequential search, binary search<br>Sort: Different types: bubble sort, selection sort, insertion sort, merge sort, quick sort, radix sort,<br>heap sort           |  |           |  |  |
| Unit 5: Trees:  |  |           |  |  |
| Basic terminology, binary tree and its representation, binary tree traversal methods, binary search tree, AVL tree, B tree, B+ tree, Heaps and its operations.  |  |           |  |  |
| Unit 6: Graphs:   |  | 05        |  |  |
| Basic terminology and representation of g<br>graph traversal techniques- Breadth First,   | graphs using adjacency matrix, storage representation,<br>Depth First                                  | Hrs       |  |  |

#### **Textbooks:**

- 1. Data Structure using C-A. M. Tanenbaum, Y. Langsam, M. J. Augenstein (PHI)
- 2. Data Structures- A Pseudo code Approach with C Richard F. Gilberg and Behrouz A. Forouzon, Cengage Learning, Second Edition.
- 3. Schaum's Outlines Data Structures Seymour Lipschutz (MGH), Tata McGraw-Hill.

#### **Reference books:**

- 1. Fundamentals of Data Structures Horowitz, Sahni CBS India
- 2. An introduction to data structures with Applications- Jean-Paul Tremblay, Paul. G. Soresan, Tata Mc-Graw Hill International Editions, Second Edition.

| Title of the Course: Digital Logic Design & Microprocessors<br>Course Code: UCSE0304 | L | Τ | Р | Credi<br>t |
|--|---|---|---|------------|
|  | 4 | - | - | 4          |

Course Prerequisite: Fundamentals of Electronics and Computers, Basic Number System

#### **Course Description:**

The course is designed to provide knowledge of basic arithmetic and logical operations in digital systems, different sequential and combinational logic design. The subject provides fundamentals of 8085 & 80x86 Family Microprocessors. The subject gives idea of how assembly language programming works. This course is prerequisite for hardware based courses like Computer Architecture & Organization.

#### **Course Objectives:**

1) To provide knowledge of basic arithmetic and logical operations in digital systems.

2) To provide hands on knowledge about different sequential and combinational logicdesign.3) To provide knowledge about construction & working of different microprocessors and

peripheral.

4) To provide knowledge about assembly language programming.

#### **Course Learning Outcomes:**

| СО         | After the completion of the course the student should be able to   |
|------------|--|
| CO1        | Describe working of basic digital components                       |
| CO2        | Illustrate different microprocessor operational & addressing modes |
| CO3        | Analyze changes in microprocessor evolution                        |
| <b>CO4</b> | Develop Assembly Language Programs                                 |

#### **CO Mapping:**

| CO  | PO<br>1 | PO<br>2 | PO 3 | PO<br>4 | PO 5 | PO 6 | PO<br>7 | PO<br>8 | PO<br>9 | PO<br>10 | PO<br>11 | PO<br>12 | PSO1 | PSO | 2 |
|-----|---------|---------|------|---------|------|------|---------|---------|---------|----------|----------|----------|------|-----|---|
| CO1 | 3       |         |      |         |      |      |         |         |         |          |          |          | 1    |     |   |
| CO2 |         |         | 2    |         |      |      |         |         |         |          |          |          |      |     |   |
| CO3 |         | 2       |      |         |      |      |         |         |         |          |          |          |      |     |   |
| CO4 |         | 2       |      |         |      |      |         |         |         |          |          |          |      |     |   |

#### Assessments :

#### **Teacher Assessment:**

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one EndSemester Examination (ESE) having 20%, 30% and 50% weights respectively.

| Assessment | Marks |
|------------|-------|
| ISE 1      | 10    |
| MSE        | 30    |
| ISE 2      | 10    |
| ESE        | 50    |

ISE 1 and ISE 2 are based on quiz / test.

| Content (normally last three modules) covered after MSE.         Course Contents:         Unit 1: Number Systems & Boolean Algebra         Analog and digital systems, representation of signed numbers, 2's complement arithmetic, BCD addition & subtraction, octal & Hexadecimal addition and subtraction, Derived gates. Reduction of Boolean expression (standard SOP & POS), simplification of boolean expression using K-map (upto 5 variable), Adders & Subtractors design using gates.         Unit 2: Combinational & Sequential Logic Design         Multiplexer, implementation of expression using MUX, Demultiplexer, decoder(74138), BCD to 7 segment decoder. Classification, Flip-flops(S-R, J-K, T, D)using gates, Race around condition Master -Slave J-K Flip Flop, Counters (Asynchronous & Synchronous), Design examples, Shift registers , State transition diagram, excitation table.         Unit 3: 8085 Microprocessor Architecture         The 8085 MPU, Microprocessor communication and bus timing, Dem ultiplexing address and Data bus, Generating control signals, The 8085 Architecture, opcode fetch machine cycle, memory read and write machine cycle. 8085 instruction groups, addressing modes.         Unit 4: 8085 Programming Techniques         Writing and execution assembly language program, counters & delays, Stack, Instructions, vectored interrupts, RIM and SIM instructions .         Basic interfacing concepts, peripherals I/O instructions IN, OUT, I/O execution, Memory - structure, interfacing & address decoding, Memory mapped I/O, I/O mapped I/O. The 8255 programmable peripheral interface, operating modes, (I/O, BSR).         Unit 5: S086 Microprocessor and Assembly Language         Architec  | MSE: Assessment is based on 50% of course content (Normally first three modules)<br>ESE: Assessment is based on 100% course content with 60-70% weightage for cour   | se         |
|--|--|------------|
| Course Contents:Unit 1:- Number Systems & Boolean Algebra<br>Analog and digital systems, representation of signed numbers, 2's complement<br>arithmetic, BCD addition & subtraction, octal & Hexadecimal addition and<br>subtraction, Derived gates. Reduction of Boolean expressions, Boolean function<br>  | content (normally last three modules) covered after MSE.   |            |
| Unit 1:- Number Systems & Boolean AlgebraAnalog and digital systems, representation of signed numbers, 2's complement<br>arithmetic, BCD addition & subtraction, octal & Hexadecimal addition and<br>subtraction, Derived gates. Reduction of Boolean expression, Boolean function<br>representation, expansion of Boolean expression (standard SOP &<br>POS),simplification of boolean expression using K-map (upto 5 variable), Adders<br>& Subtractors design using gates.Unit 2:- Combinational & Sequential Logic Design<br>Multiplexer, implementation of expression using MUX, Demultiplexer,<br>decoder(74138), BCD to 7 segment decoder. Classification, Flip-flop, Counters<br>(Asynchronous & Synchronous), Design examples, Shift registers , State transition<br>diagram, excitation table.Unit 3:- 8085 Microprocessor Architecture<br>The 8085 MPU, Microprocessor communication and bus timing, Demultiplexing<br>address and Data bus, Generating control signals, The 8085 Architecture, opcode<br>fetch machine cycle, memory read and write machine cycle. 8085 interrupt, RST<br>instruction related to stack execution of CALL and RET, The 8085 interrupt, RST<br>instructions, vectored interrupts, RIM and SIM instructions .<br>Basic interfacing concepts, peripherals I/O instructions IN, OUT, I/O execution,<br>Memory - structure, interfacing & address decoding. Memory mapped I/O, I/O<br>mapped I/O. The 8255 programmable peripheral interface, operating modes (I/O,<br>BSR).10Unit 5:- 8086 Microprocessor and Assembly Language<br>Architecture of 8086, Registers of 8086, Memory Model, Addressing Modes,<br>Instruction Set, Programming Model10Unit 6:- 80x86 Family and Pentium Microprocessors<br>The 80386 Microprocessor: The memory System, Special Pentium Registers,<br>Pentium Microprocessor : The Memory System, Special Pentium Registers,<br>Pentium Memory Management,<br>The Pentium Microprocessor : Internal st | Course Contents:   |            |
| Unit 2:- Combinational & Sequential Logic Design<br>Multiplexer, implementation of expression using MUX, Demultiplexer,<br>decoder(74138), BCD to 7 segment decoder. Classification, Flip-flops(S-R, J-<br>K,T,D)using gates, Race around condition Master –Slave J-K Flip Flop, Counters<br>(Asynchronous & Synchronous), Design examples, Shift registers , State transition<br>diagram, excitation table.8 HrUnit 3:- 8085 Microprocessor Architecture<br>The 8085 MPU, Microprocessor communication and bus timing, Demultiplexing<br>address and Data bus, Generating control signals, The 8085 Architecture, opcode<br>fetch machine cycle, memory read and write machine cycle. 8085 instruction<br>groups, addressing modes.9<br>Hrs.Unit 4:- 8085 Programming Techniques<br>Writing and execution assembly language program, counters & delays, Stack,<br>Instruction related to stack execution of CALL and RET, The 8085 interrupt, RST<br>instructions, vectored interrupts, RIM and SIM instructions IN, OUT, I/O execution,<br>Memory - structure, interfacing & address decoding. Memory mapped I/O, I/O<br>mapped I/O. The 8255 programmable peripheral interface, operating modes (I/O,<br>BSR).10<br>Hrs.Unit 6:- 80x86 Microprocessor and Assembly Language<br>Architecture of 8086, Registers of 8086, Memory Model, Addressing Modes,<br>Instruction Set, Programming Model7<br>HrUnit 6:- 80x86 Family and Pentium Microprocessors<br>The 80386 Microprocessor : The memory System, Special 80386 Registers<br>Virtual 8086 Mode, The Memory Paging Mechanism,<br>The Pentium Microprocessor : Internal structure of the Pentium Registers,<br>Pentium 4: Memory Interface, Register Set, Hyper Threading<br>Technology CPUID10<br>Hrs   | Unit 1:- Number Systems & Boolean Algebra<br>Analog and digital systems, representation of signed numbers, 2's complement<br>arithmetic, BCD addition & subtraction, octal & Hexadecimal addition and<br>subtraction, Derived gates. Reduction of Boolean expressions, Boolean function<br>representation, expansion of Boolean expression (standard SOP &<br>POS), simplification of boolean expressions using K-map (upto 5 variable), Adders<br>& Subtractors design using gates,   | 8<br>Hrs.  |
| Unit 3:- 8085 Microprocessor ArchitectureThe 8085 MPU, Microprocessor communication and bus timing, Demultiplexing<br>address and Data bus, Generating control signals, The 8085 Architecture, opcode<br>fetch machine cycle, memory read and write machine cycle. 8085 instruction<br>groups, addressing modes.9Unit 4:- 8085 Programming Techniques<br>Writing and execution assembly language program, counters & delays, Stack,<br>Instruction related to stack execution of CALL and RET, The 8085 interrupt, RST<br>instructions, vectored interrupts, RIM and SIM instructions .<br>Basic interfacing concepts, peripherals I/O instructions IN, OUT, I/O execution,<br>Memory - structure, interfacing & address decoding. Memory mapped I/O, I/O<br>mapped I/O. The 8255 programmable peripheral interface, operating modes (I/O,<br>BSR).10<br>Hrs.Unit 5:- 8086 Microprocessor and Assembly Language<br>Architecture of 8086, Registers of 8086, Memory Model, Addressing Modes,<br>Instruction Set, Programming Model7<br>HrUnit 6:- 80x86 Family and Pentium Microprocessors<br>The 80386 Microprocessor : The memory System, Special 80386 Registers<br>Virtual 8086 Mode, The Memory Paging Mechanism,<br>The Pentium Microprocessor : Internal structure of the Pentium Registers,<br>Pentium Pro Microprocessor : Internal structure of the Pentium Pro<br>The Pentium Pro Microprocessor : Internal structure of the Pentium Pro<br>The Pentium Yanagement,<br>The Pentium Pro Microprocessor : Internal structure of the Pentium Pro<br>  | Unit 2:- Combinational & Sequential Logic Design<br>Multiplexer, implementation of expression using MUX, Demultiplexer,<br>decoder(74138), BCD to 7 segment decoder. Classification, Flip-flops(S-R, J-<br>K,T,D)using gates, Race around condition Master –Slave J-K Flip Flop, Counters<br>(Asynchronous & Synchronous), Design examples, Shift registers, State transition<br>diagram, excitation table.  | 8 Hrs.     |
| Unit 4:- 8085 Programming TechniquesWriting and execution assembly language program, counters & delays, Stack,<br>Instruction related to stack execution of CALL and RET, The 8085 interrupt, RST<br>instructions, vectored interrupts, RIM and SIM instructions .10Basic interfacing concepts, peripherals I/O instructions IN, OUT, I/O execution,<br>Memory - structure, interfacing & address decoding. Memory mapped I/O, I/O<br>mapped I/O. The 8255 programmable peripheral interface, operating modes (I/O,<br>BSR).10Unit 5:- 8086 Microprocessor and Assembly Language<br>Architecture of 8086, Registers of 8086, Memory Model, Addressing Modes,<br>Instruction Set, Programming Model7 HrUnit 6:- 80x86 Family and Pentium Microprocessors<br>The 80386 Microprocessor : The memory System, Special 80386 Registers<br>Virtual 8086 Mode, The Memory Paging Mechanism,<br>The Pentium Microprocessor : The Memory System, Special Pentium Registers,<br>Pentium Memory Management,<br>The Pentium Pro Microprocessor : Internal structure of the Pentium Pro<br>The Pentium 4 : Memory Interface, Register Set, Hyper Threading<br>Technology CPUID10   | <b>Unit 3:- 8085 Microprocessor Architecture</b><br>The 8085 MPU, Microprocessor communication and bus timing, Demultiplexing<br>address and Data bus, Generating control signals, The 8085 Architecture, opcode<br>fetch machine cycle, memory read and write machine cycle. 8085 instruction<br>groups, addressing modes.  | 9<br>Hrs.  |
| Unit 5:- 8086 Microprocessor and Assembly Language<br>Architecture of 8086, Registers of 8086, Memory Model, Addressing Modes,<br>Instruction Set, Programming Model7 HrUnit 6:- 80x86 Family and Pentium Microprocessors<br>The 80386 Microprocessor: The memory System, Special 80386 Registers<br>Virtual 8086 Mode, The Memory Paging Mechanism,<br>The Pentium Microprocessor : The Memory System, Special Pentium Registers,<br>Pentium Memory Management,<br>The Pentium Pro Microprocessor : Internal structure of the Pentium Pro<br>The Pentium 4 : Memory Interface, Register Set, Hyper Threading<br>Technology CPUID10  | Unit 4:- 8085 Programming Techniques<br>Writing and execution assembly language program, counters & delays, Stack,<br>Instruction related to stack execution of CALL and RET, The 8085 interrupt, RST<br>instructions, vectored interrupts, RIM and SIM instructions .<br>Basic interfacing concepts, peripherals I/O instructions IN, OUT, I/O execution,<br>Memory - structure, interfacing & address decoding. Memory mapped I/O, I/O<br>mapped I/O. The 8255 programmable peripheral interface, operating modes (I/O,<br>BSR). | 10<br>Hrs. |
| Unit 6:- 80x86 Family and Pentium MicroprocessorsThe 80386 Microprocessor: The memory System, Special 80386 RegistersVirtual 8086 Mode, The Memory Paging Mechanism,The Pentium Microprocessor : The Memory System, Special Pentium Registers,Pentium Memory Management,The Pentium Pro Microprocessor : Internal structure of the Pentium ProThe Pentium 4 : Memory Interface, Register Set, Hyper ThreadingTechnology CPUID  | <b>Unit 5:- 8086 Microprocessor and Assembly Language</b><br>Architecture of 8086, Registers of 8086, Memory Model, Addressing Modes,<br>Instruction Set, Programming Model  | 7 Hrs.     |
|  | Unit 6:-80x86 Family and Pentium Microprocessors<br>The 80386 Microprocessor: The memory System, Special 80386 Registers<br>Virtual 8086 Mode, The Memory Paging Mechanism,<br>The Pentium Microprocessor : The Memory System, Special Pentium Registers,<br>Pentium Memory Management,<br>The Pentium Pro Microprocessor : Internal structure of the Pentium Pro<br>The Pentium 4 : Memory Interface, Register Set, Hyper Threading<br>Technology CPUID   | 10<br>Hrs. |

#### Textbooks:

- 1. Fundamental of Digital Circuits –A. Anand Kumar, 2 nd Edition, PHI Private Limited.
- 2. Microprocessor architecture, programming & applications Ramesh S. Gaonkar, New Age International publication.
- 3. Microprocessors & Interfacing: Programming & Hardware, Douglas V. Hall, Tata McGraw Hill

#### **References:**

- 1. Digital fundamentals Floyd & Jain, , Pearson education, eighth edition, 2007
- 2. Digital Design Morris Mano, Pearson Education
- 3. Modern Digital Electronics, R.P.Jain, 3rd Edition, Tata McGraw Hill, 2003
- 4. Digital systems, principles and applications Ronald Tocci, Neal S. Widmer, Gregory Moss (Pearson Education) 9th Edition.

#### Unit wise Measurable students Learning Outcomes:

After learning these Unit students will be able to-

1.1 Perform number system conversions and arithmetic operations in different number systems.

1.2 Analyze, expand or minimize boolean expression.

1.3 Use K-Map to simplify boolean expression.

2. Model different Flip-Flops and Counters.

3. Explain architectural details of 8085 microprocessor.

4.1 Classify Instruction set based on their purpose and size.

4.2 Determine addressing mode of 8085 Instructions.

4.3 Demonstrate programming skill in the assembly language programming using 8085 instruction set.

5.1 Explain architectural details of 8086 microprocessor.

5.2 Demonstrate programming skill in the assembly language programming using 8086 instruction set.

6. Analyze changes in different 80x86 family Microprocessors & Pentium Microprocessors.

| Title of the Course: Data Communication and NetworksLTP   |          |         |         |         |  |  |  |  |  |
|---|----------|---------|---------|---------|--|--|--|--|--|
| Course Code: UCSE0305   | 3        | -       | -       | 3       |  |  |  |  |  |
|   |          |         |         |         |  |  |  |  |  |
| Course Pre-Requisite:   |          |         |         |         |  |  |  |  |  |
| Course Objectives:  |          |         |         |         |  |  |  |  |  |
| 1. Help students understand basic components and devices of data communication system a                                     |          |         |         |         |  |  |  |  |  |
| 2. Study the layers in OSI and TCP/IP reference model   |          |         |         |         |  |  |  |  |  |
| 3. Study and implement the protocols and algorithms working at  | differ   | ent lay | ers in  | OSI and |  |  |  |  |  |
| TCP/IP reference models   |          |         |         |         |  |  |  |  |  |
| Course Learning Outcomes:   |          |         |         |         |  |  |  |  |  |
| Course Learning Outcomes.   |          |         |         |         |  |  |  |  |  |
| CO After the completion of the course the student should be   |          |         |         |         |  |  |  |  |  |
| able to   |          |         |         |         |  |  |  |  |  |
| <b>CO1</b> Explain the basic concepts and components of data communicat   | tion sys | tem     |         |         |  |  |  |  |  |
| <b>CO2</b> Compare and contrast various multiplexing and spreading techn  | iques a  | nd tran | ismiss  | ion     |  |  |  |  |  |
| CO3 media at physical layer   |          |         |         |         |  |  |  |  |  |
| Analyze various error detection and correction techniques at dat  | a link l | ayer    |         |         |  |  |  |  |  |
| <b>CO4</b> Classify different multiple access protocols at medium access co   | ontrol s | ublaye  | r       |         |  |  |  |  |  |
| CO BO Monning   |          |         |         |         |  |  |  |  |  |
| CO-1 O Mapping.   |          |         |         |         |  |  |  |  |  |
| CO         PO1         PO2         PO3         PO4         PO5         PO6         PO7         PO8         PO9         PO10 | PO11     | PO12    | PSO     | l PSO2  |  |  |  |  |  |
|   |          |         | 1       |         |  |  |  |  |  |
| CO1         5         1           CO2         2         3         1   |          |         | 1       |         |  |  |  |  |  |
| CO3         2         3         1           CO4         2         3         1   |          |         | 1       |         |  |  |  |  |  |
|   |          |         | 1       |         |  |  |  |  |  |
|   |          |         |         |         |  |  |  |  |  |
|   |          |         |         |         |  |  |  |  |  |
| Assessments :   |          |         |         |         |  |  |  |  |  |
| Two components of In Semester Evaluation (ISE). One Mid Semester Ex   | amina    | tion (N | ISE) ai | nd one  |  |  |  |  |  |
| End Semester Examination (ESE) having 20%, 30% and 50% weights re   | spectiv  | ely.    | 10 L) u |         |  |  |  |  |  |
| Assessment Marks  |          |         |         |         |  |  |  |  |  |
| ISE 1 10  |          |         |         |         |  |  |  |  |  |
| MSE 30  |          |         |         |         |  |  |  |  |  |
| IDE 2         IU           FSE         50   |          |         |         |         |  |  |  |  |  |
| ISE 1 and ISE 2 are based on Online objective test and guiz.  |          |         |         |         |  |  |  |  |  |
| MSE: Assessment is based on 50% of course content (Normally first three modules)  |          |         |         |         |  |  |  |  |  |
| ESE: Assessment is based on 100% course content with 60-70% weighta   | ge for   | course  | conter  | nt      |  |  |  |  |  |
| (normally last three modules) covered after MSE.  |          |         |         |         |  |  |  |  |  |
| Course Contents:  |          |         |         |         |  |  |  |  |  |
| Unit 1: Introduction  |          |         |         | o Hrs.  |  |  |  |  |  |
| 1.2 Network Hardware  |          |         |         |         |  |  |  |  |  |
| 1 3 Network Software  |          |         |         |         |  |  |  |  |  |
|   |          |         | I       |         |  |  |  |  |  |

| 1.4 Reference Models   |        |
|--|--------|
| Unit 2:- Communication Basics  | 8 Hrs. |
| 2.1 Data & Signals :- Analog & Digital, Periodic analog signals, digital signals,    |        |
| Transmission Impairments, Data rate limits & Performance                             |        |
| 2.2 Digital Transmission :- Line coding & line coding schemes (Unipolar, polar &     |        |
| bipolar) Transmission modes  |        |
|  |        |
| Unit3 :- Multiplexing and Spreading  | 7 Hrs. |
| 3.1 Multiplexing: Frequency-Division multiplexing, Wavelength-Division multiplexing, |        |
| Synchronous Time-Division multiplexing, Statistical Time-Division multiplexing       |        |
| 3.2 Spread Spectrum: Frequency Hopping Spread spectrum(FHSS), Direct Sequence        |        |
| Spread Spectrum  |        |
| Unit 4: Transmission Media   | 7 Hrs. |
| 4.1 Transmission media :- Guided, Unguided media                                     |        |
| 4.2 Network Hardware components: - Transceivers & media converters, Repeaters, NIC & |        |
| PC cards, Bridges, switches, Routers   | 0.11   |
| Unit 5: Data Link Control Layer  | 8 Hrs. |
| 4.1 Error Detection and Correction   |        |
| 4.2 Block Coding, Linear Block Codes   |        |
| 4.3 Cyclic Codes   |        |
| 4.4 Checksum   |        |
| 4.5 Data Link Control: Framing   |        |
| 4.6 Flow and Error Control   |        |
| 4.7 Protocols: Noiseless channels, Noisy Channels                                    |        |
| Unit 6: The Medium Access Control Sublayer   | 6 Hrs  |
| 5.1 Channel allocation Problem   |        |
| 5.2 Multiple Access Protocols: ALHOA, CSMA   |        |
| 5.3 Collision free protocols   |        |
| 5.4 Limited contention protocols.  |        |
| Taythooks  |        |
| 1 Data Communications and Networking – Behrouz A Forouzan (The McGraw Hill)          | (Unit  |
| 2.3.4.5)   | (enit  |
| 2. Computer Networks – Andrew S. Tanenbaum- (Prentice Hall) 5th Edition (Unit 1,     | 6)     |
| References:  | ,      |
|  |        |
| 1. Computer communications and Networking Technologies – Michael A Gallo             |        |
| (Cengage Learning)   |        |
| 2. Data & computer communications:- William Stallings (Pearson Education).           |        |
| 3. Data communication and computer Networks Ajit Pal (PHI Learning).                 |        |

|  |   | _        |   |   |        |  |  |  |  |
|--|---|----------|---|---|--------|--|--|--|--|
| Title o                                    | f the Course: Digital Logic Design & Microprocessors  | L        | Т | P | Credit |  |  |  |  |
| Lab  |   | 0        | 0 | 2 | 1      |  |  |  |  |
| Course                                     | e Code: UCSE0331  | v        | v | _ | -      |  |  |  |  |
| Course                                     | Course Prerequisite: Digital Logic Design & Microprocessors   |          |   |   |        |  |  |  |  |
| Course<br>Microp                           | Course Description: This subject covers practical details of subject Digital Logic Design & Microprocessors.  |          |   |   |        |  |  |  |  |
| Course<br>1. To pr<br>2. To pr<br>3. To pr | Course Objectives:<br>1. To provide hands on experience on construction of basic digital logic circuits<br>2. To provide knowledge about assembly language programming using 8085 instruction set.<br>3. To provide knowledge about assembly language programming using 8086 instruction set. |          |   |   |        |  |  |  |  |
| Course Learning Outcomes:                  |   |          |   |   |        |  |  |  |  |
| CO   | CO After the completion of the course the student should be   |          |   |   |        |  |  |  |  |
|  | able to   |          |   |   |        |  |  |  |  |
| <b>CO1</b>                                 | Model basic digital circuits  |          |   |   |        |  |  |  |  |
| CO2  | Develop simple assembly language programs using 8085 instruction set  |          |   |   |        |  |  |  |  |
| <b>CO3</b>                                 | Develop simple assembly language programs using 8086 instruct   | tion set | ţ |   |        |  |  |  |  |

### **CO-PO Mapping:**

| CO         | PO<br>1 | <b>PO</b><br>2 | PO<br>3 | PO<br>4 | PO<br>5 | PO<br>6 | <b>PO</b><br>7 | PO<br>8 | PO<br>9 | PO<br>10 | PO<br>11 | PO<br>12 | PSO<br>1 | PSO<br>2 |
|------------|---------|----------------|---------|---------|---------|---------|----------------|---------|---------|----------|----------|----------|----------|----------|
| CO1        | 2       |                |         |         |         |         |                |         |         |          |          |          | 1        |          |
| CO2        |         | 2              |         |         |         |         |                |         |         |          |          |          |          |          |
| <b>CO3</b> |         | 2              |         |         |         |         |                |         |         |          |          |          |          |          |

#### Assessments :

#### **Teacher Assessment:**

One component of In Semester Evaluation (ISE) and one End Semester Examination (ESE) having 50%, and 50% weights respectively.

| Assessment                                 | Marks  |
|--|--|
| ISE  | 25   |
| ESE  | 50   |
| ISE are based on practical performed/ Quiz | / Mini-Project assigned/ Presentation/ Group |

Discussion/Internal oral etc.

ESE: Assessment is based on oral examination

**Course Contents:** 

| Experiment No. 1: | : Study | of Ba | asic & | Univ | ersal | Gates | 5   |
|-------------------|---------|-------|--------|------|-------|-------|-----|
|                   | •\ T T  | 1 /   | 1      | 1 •  | C 1   | •     | . / |

| Experiment No. 1. Study of basic & Oniversal Gates                     |        |
|--|--------|
| Aim and Objectives:i) Understand working of basic gates (OR, AND, NOT) | 2 Hrs. |
| ii) Understand working of universal gates (NOR, NAND)                  |        |
| iii) Construct any gate using universal gates.                         |        |

| outcomes. Students will be use to construct thui use for busic, universal gues   |                                      |
|--|--------------------------------------|
| Theoretical Background: Logic Gates Characteristics  |                                      |
| <b>Experimentation:</b> i) Test different binary inputs to basic gates and observe the   |                                      |
| behaviour from output.   |                                      |
| ii) Construct basic gate using universal gates   |                                      |
| Results and Discussions: i)Truth Table for basic logic gates.  |                                      |
| ii) Truth-Table for universal gates  |                                      |
| iii) Compare Truth-Table of constructed circuit.   |                                      |
| <b>Conclusion:</b> i)We can verify characteristics of basic logic gates  |                                      |
| ii) We can construct any basic gate using universal gate   |                                      |
| Experiment No. 2:-Study of Boolean algebra & De Morgan's theorem   | 2 Hrs.                               |
| Aim and Objectives: Understand Boolean algebra & De Morgan's theorem   |                                      |
| Outcomes: Students will be able to demonstrate De Morgan's theorem   |                                      |
| Theoretical Background: Boolean algebra & De Morgan's theorem  |                                      |
| <b>Experimentation:</b> Construct circuit to verify De Morgan's theorem using gates.   |                                      |
| <b>Results and Discussions:</b> Truth-Table for Boolean expression to verify De-   |                                      |
| -Morgan's theorem.   |                                      |
| <b>Conclusion:</b> De Morgan's theorem is proved using Truth-Table   |                                      |
| Experiment No. 3:-Study of R-S and J-K flip-flops  | 2 Hrs.                               |
| Aim and Objectives: Construct R-S and J-K flip-flops   |                                      |
| <b>Outcomes:</b> Students will be able to implement R-S and J-K flip-flops   |                                      |
| <b>Theoretical Background:</b> Characteristics of different Flip-Flops   |                                      |
| <b>Experimentation:</b> Construct R-S and J-K flip-flops   |                                      |
| <b>Results and Discussions:</b> Truth Tables for R-S and J-K flip-flops  |                                      |
| <b>Conclusion:</b> Implemented circuit for R-S and J-K flip-flop   |                                      |
|  |                                      |
| Experiment No.4:- Study of Counters  | 2 Hrs.                               |
| <b>Experiment No.4:- Study of Counters</b><br><b>Aim and Objectives:</b> Implementing UP and DOWN counter  | 2 Hrs.                               |
| <b>Experiment No.4:- Study of Counters</b><br><b>Aim and Objectives:</b> Implementing UP and DOWN counter<br><b>Outcomes:</b> Students will be able to implement UP and DOWN counter   | 2 Hrs.                               |
| <b>Experiment No.4:- Study of Counters</b><br><b>Aim and Objectives:</b> Implementing UP and DOWN counter<br><b>Outcomes:</b> Students will be able to implement UP and DOWN counter<br><b>Theoretical Background:</b> Characteristics and types of counter  | 2 Hrs.                               |
| <b>Experiment No.4:- Study of Counters</b><br><b>Aim and Objectives:</b> Implementing UP and DOWN counter<br><b>Outcomes:</b> Students will be able to implement UP and DOWN counter<br><b>Theoretical Background:</b> Characteristics and types of counter<br><b>Experimentation:</b> ConstructUP and DOWN counter  | 2 Hrs.                               |
| <b>Experiment No.4:- Study of Counters</b><br><b>Aim and Objectives:</b> Implementing UP and DOWN counter<br><b>Outcomes:</b> Students will be able to implement UP and DOWN counter<br><b>Theoretical Background:</b> Characteristics and types of counter<br><b>Experimentation:</b> ConstructUP and DOWN counter<br><b>Results and Discussions:</b> Truth Tables for UP and DOWN counter  | 2 Hrs.                               |
| Experiment No.4:- Study of Counters<br>Aim and Objectives: Implementing UP and DOWN counter<br>Outcomes: Students will be able to implement UP and DOWN counter<br>Theoretical Background: Characteristics and types of counter<br>Experimentation: ConstructUP and DOWN counter<br>Results and Discussions: Truth Tables for UP and DOWN counter<br>Conclusion: Implemented circuit for UP and DOWN counter   | 2 Hrs.                               |
| Experiment No.4:- Study of Counters<br>Aim and Objectives: Implementing UP and DOWN counter<br>Outcomes: Students will be able to implement UP and DOWN counter<br>Theoretical Background: Characteristics and types of counter<br>Experimentation: ConstructUP and DOWN counter<br>Results and Discussions: Truth Tables for UP and DOWN counter<br>Conclusion: Implemented circuit for UP and DOWN counter<br>Experiment No.5:-Interfacing counter circuit with seven segment display  | 2 Hrs.                               |
| Experiment No.4:- Study of CountersAim and Objectives: Implementing UP and DOWN counterOutcomes: Students will be able to implement UP and DOWN counterTheoretical Background: Characteristics and types of counterExperimentation: ConstructUP and DOWN counterResults and Discussions: Truth Tables for UP and DOWN counterConclusion: Implemented circuit for UP and DOWN counterExperiment No.5:-Interfacing counter circuit with seven segment displayAim and Objectives: Interfacing counter circuit and seven segment display   | 2 Hrs.                               |
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| <ul> <li>Experiment No.4:- Study of Counters</li> <li>Aim and Objectives: Implementing UP and DOWN counter</li> <li>Outcomes: Students will be able to implement UP and DOWN counter</li> <li>Theoretical Background: Characteristics and types of counter</li> <li>Experimentation: ConstructUP and DOWN counter</li> <li>Results and Discussions: Truth Tables for UP and DOWN counter</li> <li>Conclusion: Implemented circuit for UP and DOWN counter</li> <li>Experiment No.5:-Interfacing counter circuitwith seven segment display</li> <li>Aim and Objectives: Interfacing counter circuit and seven segment display</li> <li>Outcomes: Students will be able to connect counter circuit to seven segment display</li> <li>Outcomes: Students will be able to connect circuit and seven segment display</li> <li>Results and Discussions: Observation of output on seven segment display</li> <li>Results and Discussions: Observation of output on seven segment display</li> <li>Experiment No.6:-Realization of 4/5 variable K-maps</li> <li>Aim and Objectives: Minimizing 4/5 variable expression using K-Map</li> <li>Outcomes: Students will be able to minimize 4/5 variable expression.</li> </ul>  | 2 Hrs.<br>2 Hrs.<br>2 Hrs.           |
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| <ul> <li>Experiment No.4:- Study of Counters</li> <li>Aim and Objectives: Implementing UP and DOWN counter</li> <li>Outcomes: Students will be able to implement UP and DOWN counter</li> <li>Theoretical Background: Characteristics and types of counter</li> <li>Experimentation: ConstructUP and DOWN counter</li> <li>Results and Discussions: Truth Tables for UP and DOWN counter</li> <li>Conclusion: Implemented circuit for UP and DOWN counter</li> <li>Experiment No.5:-Interfacing counter circuitwith seven segment display</li> <li>Aim and Objectives: Interfacing counter circuit and seven segment display</li> <li>Outcomes: Students will be able to connect counter circuit to seven segment display</li> <li>Outcomes: Students will be able to connect counter circuit and seven segment display</li> <li>Theoretical Background: Working of seven segment display</li> <li>Experimentation: Build interface for counter circuit and seven segment display</li> <li>Results and Discussions: Observation of output on seven segment display</li> <li>Conclusion: Built interface for counter circuit and seven segment display</li> <li>Experiment No.6:-Realization of 4/5 variable K-maps</li> <li>Aim and Objectives: Minimizing 4/5 variable expression.</li> <li>Theoretical Background: K-Map basics, Boolean algebra, De Morgan's theorem</li> <li>Experimentation: Use the K-map method minimize expression</li> <li>Results and Discussions: Verify minimized expression with Truth-Table</li> <li>Conclusion: Byfollowing K-map. expression can be minimized</li> </ul>   | 2 Hrs.<br>2 Hrs.<br>2 Hrs.           |
| <ul> <li>Experiment No.4:- Study of Counters</li> <li>Aim and Objectives: Implementing UP and DOWN counter</li> <li>Outcomes: Students will be able to implement UP and DOWN counter</li> <li>Theoretical Background: Characteristics and types of counter</li> <li>Experimentation: ConstructUP and DOWN counter</li> <li>Results and Discussions: Truth Tables for UP and DOWN counter</li> <li>Conclusion: Implemented circuit for UP and DOWN counter</li> <li>Experiment No.5:-Interfacing counter circuitwith seven segment display</li> <li>Aim and Objectives: Interfacing counter circuit and seven segment display</li> <li>Outcomes: Students will be able to connect counter circuit to seven segment display</li> <li>Outcomes: Students will be able to connect circuit and seven segment display</li> <li>Results and Discussions: Observation of output on seven segment display</li> <li>Conclusion: Built interface for counter circuit and seven segment display</li> <li>Conclusion: Built interface for counter circuit and seven segment display</li> <li>Experiment No.6:-Realization of 4/5 variable K-maps</li> <li>Aim and Objectives: Minimizing 4/5 variable expression using K-Map</li> <li>Outcomes: Students will be able to minimize 4/5 variable expression.</li> <li>Theoretical Background: K-Map basics, Boolean algebra, De Morgan's theorem</li> <li>Experimentation: Use the K-map method minimize expression</li> <li>Results and Discussions: Verify minimized expression with Truth-Table</li> <li>Conclusion: Byfollowing K-map, expression can be minimized</li> </ul>   | 2 Hrs.<br>2 Hrs.<br>2 Hrs.           |
| <ul> <li>Experiment No.4:- Study of Counters</li> <li>Aim and Objectives: Implementing UP and DOWN counter</li> <li>Outcomes: Students will be able to implement UP and DOWN counter</li> <li>Theoretical Background: Characteristics and types of counter</li> <li>Experimentation: ConstructUP and DOWN counter</li> <li>Results and Discussions: Truth Tables for UP and DOWN counter</li> <li>Conclusion: Implemented circuit for UP and DOWN counter</li> <li>Experiment No.5:-Interfacing counter circuitwith seven segment display</li> <li>Aim and Objectives: Interfacing counter circuit and seven segment display</li> <li>Outcomes: Students will be able to connect counter circuit to seven segment display</li> <li>Outcomes: Students will be able to connect circuit and seven segment display</li> <li>Results and Discussions: Observation of output on seven segment display</li> <li>Results and Discussions: Observation of output on seven segment display</li> <li>Conclusion: Built interface for counter circuit and seven segment display</li> <li>Experiment No.6:-Realization of 4/5 variable K-maps</li> <li>Aim and Objectives: Minimizing 4/5 variable expression using K-Map</li> <li>Outcomes: Students will be able to minimize 4/5 variable expression.</li> <li>Theoretical Background: K-Map basics, Boolean algebra, De Morgan's theorem</li> <li>Experimentation: Use the K-map method minimize expression</li> <li>Results and Discussions: Verify minimized expression with Truth-Table</li> <li>Conclusion: Byfollowing K-map, expression can be minimized</li> </ul>   | 2 Hrs.<br>2 Hrs.<br>2 Hrs.           |
| <ul> <li>Experiment No.4:- Study of Counters</li> <li>Aim and Objectives: Implementing UP and DOWN counter</li> <li>Outcomes: Students will be able to implement UP and DOWN counter</li> <li>Theoretical Background: Characteristics and types of counter</li> <li>Experimentation: ConstructUP and DOWN counter</li> <li>Results and Discussions: Truth Tables for UP and DOWN counter</li> <li>Conclusion: Implemented circuit for UP and DOWN counter</li> <li>Experiment No.5:-Interfacing counter circuitwith seven segment display</li> <li>Aim and Objectives: Interfacing counter circuit and seven segment display</li> <li>Outcomes: Students will be able to connect counter circuit to seven segment display</li> <li>Outcomes: Students will be able to connect counter circuit and seven segment display</li> <li>Results and Discussions: Observation of output on seven segment display</li> <li>Results and Discussions: Observation of output on seven segment display</li> <li>Conclusion: Built interface for counter circuit and seven segment display</li> <li>Conclusion: Built interface for counter circuit and seven segment display</li> <li>Conclusion: Built interface for counter circuit and seven segment display</li> <li>Conclusion: Built interface for counter circuit and seven segment display</li> <li>Conclusion: Built interface for counter circuit and seven segment display</li> <li>Conclusion: Built interface for counter circuit and seven segment display</li> <li>Conclusion: Built interface for counter circuit and seven segment display</li> <li>Conclusion: Built interface for counter circuit and seven segment display</li> <li>Conclusion: Built interface for counter circuit and seven segment display</li> <li>Conclusion: Built interface for counter circuit and seven segment display</li> <li>Conclusion: Built interface for counter circuit and seven segment display</li> <li>Conclusion: Built interface for counter circuit and seven segment display</li> <li>Conclusion: Built interface for counter circuit and seven segment display</li> <li>Conc</li></ul> | 2 Hrs.<br>2 Hrs.<br>2 Hrs.<br>2 Hrs. |

| <b>Outcomes:</b> Students will be able to explain instructions of 8085 microprocessor<br><b>Theoretical Background:</b> Architecture & Instruction Set of 8085 microprocessor<br><b>Experimentation:</b> Use various instructions of 8085 microprocessor in simulator<br><b>Results and Discussions:</b> Table of Instructions with purpose, mnemonic & size<br><b>Conclusion:</b> Demonstrated instructions using simulator  |        |
|---|--------|
| <ul> <li>Experiment No.8:- 8085 Assembly Language Programs for - <ul> <li>A. Addition / Subtraction of two 8-bit numbers</li> <li>B. Alter contents of register in 8085</li> <li>C. Arrange no.s in ascending / descending order</li> </ul> </li> <li>Aim and Objectives: Writing simple assembly language programs (listed above)</li> <li>Outcomes: Students will be able to develop simple assembly language programs</li> <li>Theoretical Background: Instruction Set of 8085 microprocessor</li> <li>Experimentation: Develop algorithm and program for given problem statements</li> <li>Results and Discussions: Execute developed programs and note the results</li> <li>Conclusion:</li> </ul> | 2 Hrs. |
| <ul> <li>Experiment No.9:- 8085 Assembly Language Programs for -</li> <li>D. Block Transfer / Exchange</li> <li>E. Find square of numbers from 0 to 9 using table of a square</li> <li>F. Generate RST 7.5 interrupts</li> <li>Aim and Objectives: Writing simple assembly language programs (listed above)</li> <li>Outcomes: Students will be able to develop simple assembly language programs</li> <li>Theoretical Background: Instruction Set of 8085 microprocessor</li> <li>Experimentation: Develop algorithm and program for given problem statements</li> <li>Results and Discussions: Execute developed programs and note the results</li> <li>Conclusion:</li> </ul>                        | 2 Hrs. |
| <ul> <li>Experiment No.10:- 8086 Assembly Language Programs for - <ul> <li>A. Sorting an array for 8086</li> <li>B. Searching for a number or character in a string for 8086</li> </ul> </li> <li>Aim and Objectives: Writing simple assembly language programs (listed above)</li> <li>Outcomes: Students will be able to develop simple assembly language programs</li> <li>Theoretical Background: Instruction Set of 8086 microprocessor</li> <li>Experimentation: Develop algorithm and program for given problem statements</li> <li>Results and Discussions: Execute developed programs and note the results</li> </ul>  | 2 Hrs  |
| <ul> <li>Experiment No.11:- 8086 Assembly Language Programs for - <ul> <li>A. String manipulations for 8086</li> <li>B. Digital clock design using 8086</li> </ul> </li> <li>Aim and Objectives: Writing simple assembly language programs (listed above)</li> <li>Outcomes: Students will be able to develop simple assembly language programs</li> <li>Theoretical Background: Instruction Set of 8086 microprocessor</li> <li>Experimentation: Develop algorithm and program for given problem statements</li> <li>Results and Discussions: Execute developed programs and note the results</li> <li>Conclusion:</li> </ul>  | 2 Hrs  |

| <ul> <li>A. ADC and DAC</li> <li>B. Stepper Motor</li> <li>Aim and Objectives: Writing simple assembly language programs (listed above)</li> <li>Outcomes: Students will be able to develop simple assembly language programs</li> <li>Theoretical Background: Instruction Set of 8086 microprocessor</li> <li>Experimentation: Develop algorithm and program for given problem statements</li> <li>Results and Discussions: Execute developed programs and note the results</li> <li>Conclusion:</li> </ul> | 2 Hrs       |
|--|-------------|
| <ul> <li>Textbooks:</li> <li>1. Fundamental of Digital Circuits –A. Anand Kumar, 2 nd Edition, PHI Private Lir</li> <li>2. Microprocessor architecture, programming &amp; applicationsRamesh S. Gaonkar, Ne Age International publication.</li> <li>3. Microprocessors &amp; Interfacing: Programming &amp; Hardware, Douglas V. Hall, Tata</li> </ul>   | nited.<br>w |
| <ul> <li>References:</li> <li>1. Digital fundamentals Floyd &amp; Jain, , Pearson education, eighth edition, 2007</li> <li>2. Digital Design –Morris Mano, Pearson Education</li> <li>3. Modern Digital Electronics, R.P.Jain, 3rd Edition, Tata McGrawHill, 2003</li> <li>4. Digital systems, principles and applications – Ronald Tocci, Neal S. Widmer, Gree Moss (Pearson Education) 9 th Edition.</li> </ul>  | gory        |

| Title of  | the Course: Data Communication and Networking Lab L T P Credit                                   |         |            |            |            |            |            |            | Credit     |             |      |             |     |        |
|---|--|---------|------------|------------|------------|------------|------------|------------|------------|-------------|------|-------------|-----|--------|
| Course  | 2 1  |         |            |            |            |            |            |            |            | 1           |      |             |     |        |
| Course  | Course Pre-Requisite:  |         |            |            |            |            |            |            |            |             |      |             |     |        |
| Course Description: Study and implement basic techniques in data communication system |  |         |            |            |            |            |            |            |            |             |      |             |     |        |
| Course  | Obje   | ectives | 5:         |            |            |            |            |            |            |             |      |             |     |        |
| To exp  | expose students to:-   |         |            |            |            |            |            |            |            |             |      |             |     |        |
| 1.  | . Basic components of data communication system  |         |            |            |            |            |            |            |            |             |      |             |     |        |
| 2.  | Netw   | orkin   | g devic    | es and t   | opolog     | ies        |            |            |            |             |      |             |     |        |
| 3.  | Laye   | red str | ucture     | of com     | puter n    | etwork     | 8          |            |            |             |      |             |     |        |
| 4.  | Func   | tional  | ities of   | Physica    | al and I   | Data Lir   | nk Laye    | r          |            |             |      |             |     |        |
| Course  | Lear   | ning (  | Outcon     | nes:       |            |            |            |            |            |             |      |             |     |        |
|   |  |         |            |            |            |            |            |            |            |             |      |             |     |        |
| CO  | After the completion of the course the student should be   |         |            |            |            |            |            |            |            |             |      |             |     |        |
|   | able to  |         |            |            |            |            |            |            |            |             |      |             |     |        |
| CO1   | Design sample network based on organizations requirements  |         |            |            |            |            |            |            |            |             |      |             |     |        |
| CO2   | Demonstrate working of different interconnecting devices using simulation tools                  |         |            |            |            |            |            |            |            |             |      |             |     |        |
| <u>CO3</u>  | Make use of different network testing tools and commands for sample network testing and analysis |         |            |            |            |            |            | analysis   |            |             |      |             |     |        |
| CO4   | 4 Design program for framing, flow control and error correction and detection techniques using   |         |            |            |            |            |            |            |            |             |      |             |     |        |
|   | programming language   |         |            |            |            |            |            |            |            |             |      |             |     |        |
| CO-PC   | ) Mar  | ning    |            |            |            |            |            |            |            |             |      |             |     |        |
| 0010  | , 11 <b>1</b> 11   | P8      |            |            |            |            |            |            |            |             |      |             |     |        |
| CO  | PO   | PO      | <b>PO3</b> | <b>PO4</b> | <b>PO5</b> | <b>PO6</b> | <b>PO7</b> | <b>PO8</b> | <b>PO9</b> | <b>PO10</b> | PO11 | <b>PO12</b> | PSO | 1 PSO2 |
|   | 1  | 2       |            |            |            |            |            |            |            |             |      |             |     |        |
| CO1   |  |         | 2          | 1          |            | 1          |            | 1          |            |             |      |             |     |        |
|   |  |         |            | -          |            | -          |            | -          |            |             |      |             |     |        |
| CO2   |  |         |            |            | 3          |            |            | 1          |            |             |      |             | 2   |        |

 CO4
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# Assessments :

**CO3** 

Teacher Assessment:

One components of In Semester Evaluation (ISE) and one End Semester Examination (ESE) having 50% and 50% weights respectively.

1

| Marks | Assessment |
|-------|------------|
| 25    | ISE        |
| 50    | ESE(POE)   |

**Course Contents:** 

Experiment No. 1:- Campus Network Design using CISCO Packet Tracer

2

| Experiment No. 2:- Demonstration of Interconnecting Devices using CISCO Packet Tracer           |       |
|---|-------|
| Experiment No.3:- Study of connectivity test tools with all its option                          | 2 Hrs |
| Experiment No. 4:- Wireshark Network Protocol Analyzer  | 2 Hrs |
| Experiment No. 5:- Design and Implementation of Framing Techniques                              | 2 Hrs |
| A) Character Count  |       |
| B) Bit Stuffing   |       |
| Experiment No. 6:- Design and Implementation of Error Detection and Correction Codes            | 2 Hrs |
| A) Cyclic Redundancy Check  |       |
| B) Hamming Code   |       |
| Experiment No. 7:- Design and Implementing Elementary data link protocol (Stop & wait protocol) | 2 Hrs |
| Experiment No. 8:- Design and Implementing Elementary data link protocol (Go Back N)            | 2 Hrs |
| Experiment No. 9:- Design and Implementing Elementary data link protocol (Selective Repeat)     | 2 Hrs |

| Course Code: UCSE0333       -  | s.<br>eues, Trees of<br>Lists, Link  | etc.                 | 2<br>Queues, |  |  |  |  |  |
|--|--|----------------------|--------------|--|--|--|--|--|
| Course Pre-requisite: Computer Programming         Course Objectives:         1. To learn basic concepts of C language structures, Arrays, lists pointers         2. To become familiar with advanced data structures such as Stacks, Que         3. To analyze and solve problems using advanced data structures such as Stacks, Trees, and Graphs.         4. To write programs on Linked Lists, Doubly Linked Lists, Trees etc.         Course Outcomes:         Co         After completion of the course a student should be able to:         Define the basic terms of Linear Lists. Linked List. Doubly Linked  | s.<br>eues, Trees (<br>Lists, Link   | etc.<br>ed Lists, (  | Queues,      |  |  |  |  |  |
| Course Objectives:         1. To learn basic concepts of C language structures, Arrays, lists pointers         2. To become familiar with advanced data structures such as Stacks, Que         3. To analyze and solve problems using advanced data structures such as Stacks, Trees, and Graphs.         4. To write programs on Linked Lists, Doubly Linked Lists, Trees etc.         Course Outcomes:         Co         After completion of the course a student should be able to:         Define the basic terms of Linear Lists. Linked List. Doubly Linked   | s.<br>eues, Trees (<br>Lists, Link   | etc.<br>Ted Lists, ( | Queues,      |  |  |  |  |  |
| <ol> <li>To learn basic concepts of C language structures, Arrays, lists pointers</li> <li>To become familiar with advanced data structures such as Stacks, Que</li> <li>To analyze and solve problems using advanced data structures such as Stacks, Trees, and Graphs.</li> <li>To write programs on Linked Lists, Doubly Linked Lists, Trees etc.</li> </ol> Course Outcomes:           CO         After completion of the course a student should be able to:  | s.<br>eues, Trees (<br>Lists, Link   | etc.<br>ed Lists, (  | Queues,      |  |  |  |  |  |
| <ol> <li>To become familiar with advanced data structures such as Stacks, Que</li> <li>To analyze and solve problems using advanced data structures such as Stacks, Trees, and Graphs.</li> <li>To write programs on Linked Lists, Doubly Linked Lists, Trees etc.</li> </ol> Course Outcomes:           CO         After completion of the course a student should be able to:  | eues, Trees (<br>Lists, Link   | etc.<br>ed Lists, (  | Queues,      |  |  |  |  |  |
| <ul> <li>3. To analyze and solve problems using advanced data structures such as Stacks, Trees, and Graphs.</li> <li>4. To write programs on Linked Lists, Doubly Linked Lists, Trees etc.</li> </ul> Course Outcomes:   CO After completion of the course a student should be able to:  | Lists, Link  | ed Lists, (          | Queues,      |  |  |  |  |  |
| Stacks, Trees, and Graphs.         4. To write programs on Linked Lists, Doubly Linked Lists, Trees etc.         Course Outcomes:         CO       After completion of the course a student should be able to:         Define the basic terms of Linear Lists       Linked List  |  |                      |              |  |  |  |  |  |
| <ul> <li>4. To write programs on Linked Lists, Doubly Linked Lists, Trees etc.</li> <li>Course Outcomes:</li> <li>CO After completion of the course a student should be able to:</li> </ul>  |  |                      |              |  |  |  |  |  |
| Course Outcomes:         CO       After completion of the course a student should be able to:         Define the basic terms of Linear Lists       Linked List   |  |                      |              |  |  |  |  |  |
| CO After completion of the course a student should be able to:   |  |                      |              |  |  |  |  |  |
| CO       After completion of the course a student should be able to:         Define the basic terms of Linear Lists       Linked List  |  |                      |              |  |  |  |  |  |
| Define the basic terms of Linear Lists Linked List Doubly Linked   |  |                      |              |  |  |  |  |  |
| Define the basic terms of Linear Lists Linked List Doubly Linked   |  |                      |              |  |  |  |  |  |
| Define the basic terms of Linear Lists, Linked List, Doubly Linked   | d List, Non  | Linear D             | ata          |  |  |  |  |  |
| CO1<br>Structures( Binary Trees, AVL Trees, Graphs )   |  |                      |              |  |  |  |  |  |
| <b>CO 2</b> Choose the appropriate and optimal data structure for a specified a  | <b>O</b> ? Choose the appropriate and optimal data structure for a specified application |                      |              |  |  |  |  |  |
| Choose the appropriate and optimal data structure for a specified application  |  |                      |              |  |  |  |  |  |
| <b>CO 3</b> Write programs and applications with Static and Dynamic data stru  | CO 3Write programs and applications with Static and Dynamic data structures              |                      |              |  |  |  |  |  |
| Mapping of course outcomes with program outcomes:  |  |                      |              |  |  |  |  |  |
|  |  |                      | <u> </u>     |  |  |  |  |  |
| COs         PO         PO | ) PO12   | PSO1                 | PSO2         |  |  |  |  |  |
|  |  |                      |              |  |  |  |  |  |
| CO1 3  |  | 1                    | 1            |  |  |  |  |  |
| <b>CO2</b> 3   |  | 1                    | 1            |  |  |  |  |  |
| CO3 2  |  | +                    | 2            |  |  |  |  |  |

#### Assessment:

#### **Teacher Assessment:**

One component of In Semester Evaluation (ISE) and one End Semester Examination (ESE) having 50% and 50% weight age respectively.

| Assessment | Marks |
|------------|-------|
| ISE        | 50    |
| ESE(POE)   | 50    |

#### **Course Contents:**

#### Assignments based on topics covered in course UCSE0303 Data Structures:

- 1. Program based on arrays, structures and pointers.
- 2. Program based on functions and recursion.
- 3. Program for developing an application using stack.
- 4. Program for developing an application using queue and circular queue.
- 5. Program for developing an application using singly linked list.
- 6. Program for developing an application using doubly linked list.
- 7. Program for developing an application using circularly linked list.
- 8. Program based on implementation of hashing and rehashing.
- 9. Program based on implementation of linear search, binary search.
- 10. Program based on one of the sorting techniques.
- 11. Program based on one of the sorting techniques.
- 12. Implementation of recursive and non-recursive tree traversals.
- 13. Implementation of basic binary search tree and its application.
- 14. Program based on AVL tree / B-tree.
- 15. Program based on representation of graphs
- 16. Program based on DFS and BFS search.

#### **Textbooks:**

- 1. Data Structures- A Pseudo code Approach with C Richard F. Gilberg and Behrouz A. Forouzon, Cengage Learning, Second Edition.
- 2. Schaum's Outlines Data Structures Seymour Lipschutz (MGH), Tata McGraw-Hill.
- 3. The C Programming langauge Kernighan and Ritchie

## **Reference books:**

- 1. Data Structure using C- A. M. Tanenbaum, Y. Langsam, M. J. Augenstein (PHI)
- 2. An introduction to data structures with Applications- Jean-Paul Tremblay, Paul. G. Soresan, Tata Mc-Graw Hill International Editions, Second Edition.

# **SEM-II**

| Title of the Course: Automata Theory   L   T   P   Credit   |   |                        |               |            |            |            |                |            | redit             |             |            |           |          |            |
|---|---|------------------------|---------------|------------|------------|------------|----------------|------------|-------------------|-------------|------------|-----------|----------|------------|
| Course Code: UCSE0401   |   |                        |               |            |            |            |                |            |                   | 3           | 1          |           | 4        |            |
| Course  | Pre-R   | equisit                | e: Disci      | rete Ma    | athema     | tics, So   | ets, Ca        | rtesian    | Produc            | et and F    | unction    | 5         |          |            |
| Course  | <b>Course Description:</b> This course deals with the theoretical background of computer science. |                        |               |            |            |            |                |            |                   |             |            |           |          |            |
| Course Objectives:  |   |                        |               |            |            |            |                |            |                   |             |            |           |          |            |
| 1. To expose the students to the mathematical foundations and principles of computer science      |   |                        |               |            |            |            |                |            |                   |             |            |           |          |            |
| 2. To strengthen the students' ability to carry out formal and higher studies in computer science |   |                        |               |            |            |            |                |            |                   |             |            |           |          |            |
| 3. To make the students understand the use of automata theory in Compliers & System programming.  |   |                        |               |            |            |            |                |            |                   |             |            |           |          |            |
| 4. To make the student aware of mathematical tools, formal methods & automata techniques for      |   |                        |               |            |            |            |                |            |                   |             |            |           |          |            |
| compu   | computing.  |                        |               |            |            |            |                |            |                   |             |            |           |          |            |
| Course  | e Lear  | ning ()                | outcon        | nes:       |            |            |                |            |                   |             |            |           |          |            |
|   |   |                        |               |            |            |            |                |            |                   |             |            |           |          |            |
| CO  | Aftor   | the of                 | mnlot         | ion of     | the co     | urco tl    | a stud         | lant ch    | ould b            | o oblo t    | 0          |           |          |            |
| co  | Alter   | the co                 | mpier         | 1011 01    | the co     | ui se u    | ie stuu        | ient sn    |                   | e able t    | 0          |           |          |            |
| <u>CO1</u>  | <b>F</b> 1  | • • • • • • • • •      |               |            |            |            | 1.4            | 4          |                   |             |            |           |          |            |
| $\frac{CO1}{CO2}$   | Expla   | ain type               | es of I       | ormal I    | angua      | ges and    | 1 their        | accepto    | ors               |             |            |           |          |            |
| C02   | Dalat   | a tha a                |               | iguage     | es on un   | le Dasis   | the me         | odorna     | ures              | anutant     | ashnala    | aiaa      |          |            |
| CO3   | Desis   |                        | mput          |            | mode       | is with    | me me          |            |                   | fied pro    | bloma      | gies      |          |            |
| C04   | Desig   | gn com                 | putatio       | onal ma    | achine     | s or va    | rious t        | ypes I c   | or speci          | ned pro     | biems      |           |          |            |
| CO-PO Mapping:  |   |                        |               |            |            |            |                |            |                   |             |            |           |          |            |
| CO  | <b>PO1</b>  | <b>PO2</b>             | <b>PO3</b>    | <b>PO4</b> | <b>PO5</b> | <b>PO6</b> | <b>PO7</b>     | <b>PO8</b> | <b>PO9</b>        | <b>PO10</b> | PO11       | PO12      | PSO1     | PSO2       |
| <b>CO1</b>  | 2   |                        |               |            |            |            |                |            |                   |             |            |           |          |            |
| CO2   | 2   |                        |               |            |            |            |                |            |                   |             |            |           |          |            |
| <b>CO3</b>  |   | 2                      |               |            |            |            |                |            |                   |             |            |           |          | 1          |
| <b>CO4</b>  |   |                        | 3             |            |            |            |                |            |                   |             |            |           |          | 1          |
| Assess<br>Teache<br>Two co  | ments<br>er Asso<br>ompon   | :<br>essmer<br>ents of | nt:<br>In Ser | nester     | Evalua     | ation (I   | SE), O         | ne Mic     | l Seme            | ster Exa    | minatio    | on (MSE   | ) and o  | ne         |
| EndSer  | nester  | Exami                  | ination       | (ESE)      | havin      | g 20%,     | <u>, 30% a</u> | and 50     | % weig            | hts resp    | ectively   | · .       |          |            |
| Asses   | sment   |                        |               |            |            |            | Mark           | .s         |                   |             |            |           |          |            |
| ISE I   |   |                        |               |            |            |            | 10             |            |                   |             |            |           |          |            |
| MSE   |   |                        |               |            |            |            | 30             |            |                   |             |            |           |          |            |
| ISE 2   |   |                        |               |            |            |            | 10             |            |                   |             |            |           |          |            |
| ESE   |   |                        |               |            |            |            | 50             |            | , -               | 10          | <u>.</u> . |           |          |            |
| ISE 1 a   | nd ISE  | $\pm 2 \text{ are}$    | based         | on assi    | gnmer      | nt/decla   | ared te        | st/quiz    | /semina           | ar/Grou     | p Discus   | ssions et | c.       |            |
| MSE: A  | Assess  | ment is                | based         | on 50      | % of c     | oursec     | ontent         | (Norn      | nally fii<br>700/ | rst three   | module     | es)       |          | 11         |
| ESE: A  | ssessn  | nent is $1 - 1$        | based         | on $100$   | J% COU     | rsecoi     | ntent w        | 111160-    | /U% W             | eightage    | e Ior co   | urse con  | tent (no | ormally    |
| last three modules) covered after MSE.  |   |                        |               |            |            |            |                |            |                   |             |            |           |          |            |
| Course Contents:  |   |                        |               |            |            |            |                |            |                   |             |            |           |          |            |
| UNII-   |   |                        | ucal I        |            | on, Ke     | gular      |                | ages d     | x r mito          | e Auton     |            |           | vð Hr    | <b>'S.</b> |
| I ne Pri  | nciple  | oi Ma                  | tnemat        | ical In    | ductio     | n Kecu     | rsive I        | Jefiniti   | ions, De          | eminitio    | n & ty     | pes of    |          |            |
|   |   |                        |               |            |            |            |                |            |                   |             |            |           |          |            |

| grammars & languages, Regular expressions and corresponding regular languages,                              |                         |  |  |  |  |  |  |
|---|-------------------------|--|--|--|--|--|--|
| examples and applications, unions, intersection & complements of regular languages,                         |                         |  |  |  |  |  |  |
| Finite automata-definition and representation, on-deterministic F.A.,NFA with null                          |                         |  |  |  |  |  |  |
| transitions, Equivalence of FA's, NFA's and NFA's with null transitions.                                    |                         |  |  |  |  |  |  |
| UNIT-II: Kleene's Theorem:  | 04 Hrs.                 |  |  |  |  |  |  |
| Part I & II statements and proofs, minimum state of FA for a regular language,                              |                         |  |  |  |  |  |  |
| minimizing number of states in Finite Automata.   |                         |  |  |  |  |  |  |
| UNIT-III: Grammars and Languages:   | 10 Hrs.                 |  |  |  |  |  |  |
| Derivation and ambiguity, BNF & CNF notations, Union, Concatenation and *'s of                              |                         |  |  |  |  |  |  |
| CFLs, Eliminating production & unit productions from CFG, Eliminating useless                               |                         |  |  |  |  |  |  |
| variables from a context Free Grammar. Parsing: Top-Down, Recursive Descent and                             |                         |  |  |  |  |  |  |
| Bottom-Up Parsing   |                         |  |  |  |  |  |  |
| UNIT-IV: Push Down Automata   | 04 Hrs.                 |  |  |  |  |  |  |
| Definition, Deterministic PDA & types of acceptance, Equivalence of CFG's & PDA's.                          |                         |  |  |  |  |  |  |
| UNIT-V: CFL's and non CFL's :   | 04 Hrs.                 |  |  |  |  |  |  |
| Pumping Lemma and examples, intersections and complements.  |                         |  |  |  |  |  |  |
| UNIT-VI: Turing Machines: Models of computation, definition of Turing Machine as                            | 10 Hrs.                 |  |  |  |  |  |  |
| Language acceptors, combining Turing Machines, Computing a function with a TM,                              |                         |  |  |  |  |  |  |
| Non-deterministic TM and Universal TM, Recursively enumerable languages,                                    |                         |  |  |  |  |  |  |
| Unsolvable problems.  |                         |  |  |  |  |  |  |
| Textbooks:  |                         |  |  |  |  |  |  |
| 1. Introduction to languages & Theory of computations – John C. Martin (MGH) – Chapters                     | 1, 2, 3, 4, 5, 6, 7, 8. |  |  |  |  |  |  |
| 2. Discrete Mathematical Structures with applications to Computer Science-J.P.Trembley                      | & R.Manohar             |  |  |  |  |  |  |
| (MGH) Chapter 1,  |                         |  |  |  |  |  |  |
|   |                         |  |  |  |  |  |  |
| References:   |                         |  |  |  |  |  |  |
| 1.Introduction to Automata Theory, Languages and computation – John E. Hopcraft, Rajeev Motwani, Jeffrey D. |                         |  |  |  |  |  |  |
| Uliman (Pearson Edition).   |                         |  |  |  |  |  |  |
| 2. Introduction to Theory of Computations – Michael Sipser (Thomson Brooks / Cole)                          |                         |  |  |  |  |  |  |
| 3 Theory Of Computation-Vivek Kulkarni 1st edition OXFORD university Press                                  |                         |  |  |  |  |  |  |

4. Theory Of Computation A problem Solving Approach Kavi Mahesh Wiley India

| Title o   | tle of the Course: Computer Graphics L T P   |           |                |                |         |          |           |         |         |           |              | Credit    |        |           |
|---|--|-----------|----------------|----------------|---------|----------|-----------|---------|---------|-----------|--------------|-----------|--------|-----------|
| Cours   | e Code   | : UCSE    | 0402           |                |         |          |           |         |         |           | 3            |           |        | 3         |
| Cours   | e Pre-l  | Requisit  | :e:            |                |         |          |           |         |         |           |              |           |        |           |
| Cours   | e Desci  | ription:  | Study          | basic a        | and co  | re conc  | epts ir   | ı Comj  | puter C | Braphics  | 8            |           |        |           |
| Cours   | Lourse UDJectives:   |           |                |                |         |          |           |         |         |           |              |           |        |           |
| 1.  | To pr  | ovide st  | udents         | with a         | n unde  | erstand  | ing of    | variou  | s trans | formati   | on tech      | inique    | s and  |           |
|   |  |           |                |                | _       |          |           |         | _       |           |              |           |        |           |
| 2.  | 2. To provide students with an understanding of various algorithms related to drawing line,<br>circle polygon scanning, filling, windowing and clipping of graphical objects |           |                |                |         |          |           |         |         |           |              |           |        |           |
| circle, polygon scanning, filling, windowing and clipping of graphical objects.   |  |           |                |                |         |          |           |         |         |           |              |           |        |           |
| 3.  | 3. To provide students with an understanding of the mathematics underlying two- and three-   |           |                |                |         |          |           |         |         |           |              | nd three- |        |           |
|   | dime   | nsional   | inter          | oolatin        | g curv  | es and   | l to le   | arn th  | e War   | nock a    | nd dep       | th-buf    | fer (2 | Z-buffer) |
|   | algor  | ithm us   | ed to d        | etermi         | ne hid  | den lin  | es and    | surfac  | es in a | rendere   | ed scene     | e         | _      |           |
| 4.  | To en  | able stu  | dents t        | o acqu         | ire pra | ctical l | knowle    | edge in | anima   | tion, il  | lumina       | tion, li  | ghter  | ing and   |
|   | rende  | ring usi  | ng Ope         | enGL.          |         |          |           |         |         |           |              |           |        |           |
| Cours   | e I ear  | ning Ar   | itcome         | ×.             |         |          |           |         |         |           |              |           |        |           |
|   |  | er the c  | omple          | .s.<br>tion of | f the c | ourse f  | the stu   | ident s | should  | be abl    | e to         |           |        |           |
| 00  |  |           | ompre          |                |         | ourse    |           |         |         | be usi    |              |           |        |           |
| CO1   | Explain the basic concepts of interactive computer graphics.   |           |                |                |         |          |           |         |         |           |              |           |        |           |
| CO2   | Illustrate the core concepts of computer graphics, including viewing, projection,  |           |                |                |         |          |           |         |         |           |              |           |        |           |
|   | per  | spective  | and tr         | ansfor         | matior  | in two   | o and the | hree di | mensio  | ons.      |              |           |        |           |
| CO3   | Ap   | ply the r | nathen         | natical        | found   | ations   | to inter  | rpolate | e paran | netric ar | nd non-      | param     | etric  | curves    |
| CO4   | Δn   | alvze ba  | s.<br>sic illu | minati         | on mo   | dels ar  | nd noly   | oon re  | nderin  | o meth    | ods          |           |        |           |
| 004   | 2 111  | aryze ou  | 510 1110       | iiiiiiuu       | on mo   | ucis ui  | ia pory   | 50110   | nuerm   | ig mem    | <b>Ju</b> 5. |           |        |           |
| CO-P  | O Map  | ping:     |                |                |         |          |           |         |         |           |              |           |        |           |
| CC  | )   PC   | ) PO      | PO             | PO             | PO      | PO       | PO        | PO      | PO      | PO10      | <b>PO1</b>   | 1   PC    | P      | S PS      |
|   | 1  | 2         | 3              | 4              | 5       | 6        | 7         | 8       | 9       |           |              | 12        | 0      | 1 02      |
| CO  | 1 3  |           |                |                | 2       |          |           |         |         |           |              |           | _      |           |
|   | $\frac{1}{2}$ 3  | 3         | 2              | 1              | 2       |          |           |         |         |           |              |           | 2      | 2 3       |
| CO  | <b>3</b> 3   | 3         | 2              | 1              |         |          |           |         |         |           |              |           |        | 3 3       |
| CO  | 94   | 3         | 2              | 2              |         |          |           |         |         |           |              |           |        | 3 3       |
| Assess  | ments  | :         |                |                |         |          |           |         |         |           |              |           |        |           |
| Teach   | er Asse  | essment   | :              |                |         |          |           |         |         |           |              |           |        |           |
| Two c   | ompon  | ents of I | n Sem          | ester E        | valuat  | ion (IS  | E), Or    | ne Mid  | Semes   | ster Exa  | minati       | on (M     | SE) a  | nd one    |
| EndSe   | mester   | Examir    | ation (        | ESE) I         | naving  | 20%,     | 30% ai    | nd 50%  | 6 weig  | hts resp  | ectivel      | у.        |        |           |
| Asses   | ssment   |           |                |                |         |          | N         | larks   |         |           |              |           |        |           |
| ISE I   |  |           |                |                |         |          | 10        | )       |         |           |              |           |        |           |
| MSE   |  |           |                |                |         |          | 30        | )       |         |           |              |           |        |           |
| ISE 2   | 2  |           |                |                |         |          | 10        | )       |         |           |              |           |        |           |
| ESE   | 1101   | 10 1      | 1              | 0.1            | 1.      |          | 50        | )       | •       | •         |              |           |        |           |
| ISE 1 :   | and ISE  | 2 2 are b | ased of        | n Onlii $500'$ | ne obje | ctive t  | est, pro  | esentat | 10n, se | minar,    | quiz ete     | c.        |        |           |
| MSE:  | MSE: Assessment is based on 50% of course content (Normally first three modules)   |           |                |                |         |          |           |         |         |           |              |           |        |           |
| LOE. Assessment is based on 100% course content with 60-70% Weightage for course content<br>(normally last three modules) covered after MSE |  |           |                |                |         |          |           |         |         |           |              |           |        |           |
| Course Contents:  |  |           |                |                |         |          |           |         |         |           |              |           |        |           |
| Unit 1  | : Intro  | duction   | 1              |                |         |          |           |         |         |           |              |           |        | 6 Hrs.    |
| 1.1 Ov  | verview  | of grap   | hics sy        | stems          | – Vide  | eo disp  | lay dev   | vices,  |         |           |              |           |        |           |
| 1.2 Ra  | ster sca   | an syster | ns             |                |         |          |           |         |         |           |              |           |        |           |

| 1.3 Random scan systems   |          |
|---|----------|
| 1.4 Graphics monitors and Workstations,   |          |
| 1.5 Input devices, Hard copy Devices, Graphics Software                                   |          |
|   | 8 Hrs.   |
| Unit 2 : Transformations  |          |
| 2.1 Basic 2D & 3D transformations - Translation, Scaling, Rotation, Reflection, Shearing, |          |
| Multiple Transformations  |          |
| 2.2 Rotation about an axis parallel to a coordinate axis                                  |          |
| 2.3 Rotation about an arbitrary axis in space   |          |
| 2.4 Affine and Perspective Geometry   |          |
| 2.5 Orthographic projections  |          |
| 2.6 Axonometric projections.  |          |
|   | 8 Hrs.   |
| Unit 3. Paster Scan Cranhies  |          |
| 3.1 Bresenhams Line drawing algorithm   |          |
| 3.2 Bresenhams Circle drawing algorithm   |          |
| 3.3 Scan Conversion techniques: RLF Frame Buffer  |          |
| 3.4 Scan converting polygons: Edge fill and Seed fill algorithms                          |          |
| 3.4 Scar converting polygons. Edge fin and Seed fin argorithms                            |          |
| 5.5 Anti-anasing  | 1 Hrs    |
| Unit 4: Viewing and clipping  | 7 111 5. |
| Onit 4: viewing and cripping  |          |
| 4.1 Introduction  |          |
| 4.2 Windowing and View-porting,   |          |
| 4.3 Sutherland - Cohen line clipping algorithm  |          |
|   | 8 Hrs.   |
| Unit 5 : Curves and Surfaces  |          |
| 5.1 Non-parametric and parametric curves  |          |
| 5.2 Representation of space curves  |          |
| 5.3 Cubic Spline  |          |
| 5.4 Parabolic Blended curves  |          |
| 5.5 Bezier curves   |          |
| 5.6 B-spline curves   |          |
| 5.7 Z- buffer algorithm   |          |
| 5.8 Warnock algorithm   |          |
|   | 8 Hrs.   |
| Unit 6 : Illumination models and surface rendering methods                                |          |
| 6.1 Light sources   |          |
| 6.2 Basic illumination models   |          |
| 6.3 Displaying light intensities  |          |
| 6.4 Halftone patterns and Dithering Techniques  |          |
| 6.5 Polygon Rendering methods   |          |
| 6.6 Ray tracing methods   |          |
|   |          |
| Textbooks:  | D 1      |

- 1. Computer Graphics C Version second edition –Donald D. Hearn, M. Pauline Baker (Pearson)
- 2. Mathematical elements for Computer Graphics David F. Rogers, J. Alan Adams (MGH

International)

3. Procedural elements for Computer Graphics - David F. Rogers (MGH International)

#### **References:**

- 1. Principles of Computer Graphics Theory and Practice Using OpenGL and Maya, Shalini Govil-Pai, (Springer).
- 2. Computer Graphics (second Edition) Zhigang Xiang & Roy Plastock (Schaum's Outline Series, TMGH).
- 3. Computer Graphics Using OpenGL F.S. Hill Jr. Stephen M. Kelley, (Pearson Education).

#### Unit Wise Measurable Students Learning Outcomes:

1 Explain the graphics devices

2 Explain 2D and 3D transformations

- 3 Explain algorithms for drawing line, circle and polygon filling
- 4 Explain algorithms for clipping and hidden line elimination
- 5 Explain mathematical representation of plane curves and space curves

6 Explain different illumination models

| Title of the Course: Computer Networks | L | Т | Р | Credit |
|--|---|---|---|--------|
| Course Code: UCSE0403                  |   |   |   |        |
|  | 3 | - | - | 3      |

#### **Course Pre-Requisite:**

UCSE0305 Data Communication and Networks

<u>Course Description</u>: This course provides a solid understanding of each of the most important networking protocols within the IP suite. The Internet protocol suite provides end-to-end data communication specifying how data should be packetized, addressed, transmitted, routed and received.

#### **Course Objectives:**

1: To make students able to identify client-server model and implement it using socket programming.

2: To introduce students with emerging protocols IPv6 and the ICMPv6 and write applications to communicate using IPv6.

3: To make students familiar with architecture and working of protocols like IP, TCP, UDP, DHCP, DNS, FTP, WWW

4: To make students able to understand working of email system and write an application to send and receive email

#### **Course Learning Outcomes:**

| СО  | After the completion of the course the student should be<br>able to                       |
|-----|---|
| CO1 | Recall the basic concept of Network, Transport and Application Layer.                     |
| CO2 | Describe different terminologies of client server programming                             |
| CO3 | Illustrate different application layer protocol like DHCP, DNS, FTP, HTTP, SMTP and SNMP. |
| CO4 | Describe various protocols supported by multimedia content.                               |

#### **CO-PO Mapping:**

| CO         | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | <b>PO7</b> | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|------------|-----|-----|-----|-----|-----|-----|------------|-----|-----|------|------|------|------|------|
| CO1        | 1   |     |     |     |     |     |            |     |     |      |      |      |      |      |
| CO2        |     |     | 2   |     |     |     |            |     |     |      |      |      | 2    |      |
| CO3        | 3   |     |     |     |     |     |            |     |     |      |      |      | 1    |      |
| <b>CO4</b> | 2   |     |     |     |     |     |            |     |     |      |      |      |      |      |

#### Assessments :

#### Teacher Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weights respectively.

| Assessment | Marks |  |  |  |  |  |  |
|------------|-------|--|--|--|--|--|--|
| ISE 1      | 10    |  |  |  |  |  |  |
| MSE        | 30    |  |  |  |  |  |  |
| ISE 2      | 10    |  |  |  |  |  |  |
| ESE        | 50    |  |  |  |  |  |  |

ISE 1 and ISE 2 are based on Online objective test and quiz. MSE: Assessment is based on 50% of course content (Normally first three modules) ESE: Assessment is based on 100% course content with 60-70% weightage for course content (normally last three modules) covered after MSE. Course Contenter

| Course Contents:   |        |
|--|--------|
| UNIT-I : : Network Layer   | 8 Hrs. |
| Introduction, Network layer services, addressing, IP packet format, ARP, RARP, ICMP, Packet  |        |
| routing protocols, congestion control, IPv6- Introduction, addressing, transition from IPv4 to   |        |
| IPVo   |        |
| UNIT-II: Transport Layer   | 8Hrs.  |
| Transport layer functions, UDP- datagram, services, applications, TCP - services, segment,   |        |
| connection, state transition diagram, Flow control, congestion control, error control, timers.   |        |
| UNIT-III: Introduction to Application Layer  | 6 Hrs. |
| Client-Server paradigm, client, server, concurrency, socket interface, communication using TCP,  |        |
| communication using UDP  |        |
| UNIT-IV: DHCP, DNS, FTP and TFTP   | 9 Hrs. |
| DHCP: Introduction, Previous Protocols, DHCP operation, Packet Format, DHCP  |        |
| Configuration. DNS: Need, Name Space, Domain Name Space, Distribution of name space, and DNS in internet. Possibilition DNS massages. Types of records. Compression examples |        |
| encapsulation, FTP: Connections, Communication, Command processing, File transfer, User  |        |
| interface, Anonymous FTP, TFTP.  |        |
|  |        |
| UNIT-V: HTTP, Electronic Mail, SNMP  | 9 Hrs. |
| HTTP: Architecture, Web Documents, HTTP Transaction, Request & Response messages: header   |        |
| & examples, Persistent vs. non persistent HTTP, Proxy Servers. Architecture, User agents,  |        |
| addresses, delayed delivery, Aliases, Mail transfer agent SMTP commands & responses, mail  |        |
| transfer phases, MIME, Mail Delivery, mail access protocols, SNMP.   | 9 Ung  |
| UNIT-VI: Multimedia in Internet:   | 0 1115 |
| Streaming stored audio/video, streaming live audio/video, real-time interactive audio/video, real-   |        |
| time transport protocol (RTP), real-time transport control protocol (RTCP), voice over IP (voiP):  |        |
| session initiation protocol (SIP) and H.323.   |        |
| Textbooks:   |        |
| 1. TCP/IP Protocol Suite by B. A. Forouzan, TMGH Publication   |        |
| References:  |        |
| 1. Computer Networks by Andrew Tanenbaum, PHI Publication  |        |
| 2. Computer Networks by William Stallings, PHI Publication   |        |

| Title of t   | he Course: Computer Organization and Architecture  | L        | Т       | Р                 | Credit      |  |  |  |  |  |  |
|--|--|----------|---------|-------------------|-------------|--|--|--|--|--|--|
| Course   | Code:UCSE0404  | 3        | -       | -                 | 3           |  |  |  |  |  |  |
| Course P   | Course Pre-Requisite: Digital Logic Design (UCSE0304), Digital Logic Design Lab (UCSE0331) |          |         |                   |             |  |  |  |  |  |  |
| <b>Course Description:</b><br>This course will introduce students to the fundamental concepts of modern computer organization and erabitecture. Course, introduces, berdware, design, basis, structure, and behavior, of the various |  |          |         |                   |             |  |  |  |  |  |  |
| architecture. Course introduces hardware design, basic structure and behavior of the various   |  |          |         |                   |             |  |  |  |  |  |  |
| It covers i  | instruction sets. CPU structure and functions memory system of                             | rganiza  | tion a  | eus or<br>1d arch | ule usel.   |  |  |  |  |  |  |
| multiproc  | essor systems. The emphasis is on studying and analyzing fund                              | amenta   | l issue | s in ar           | chitecture, |  |  |  |  |  |  |
| design an  | d their impact on performance.   |          |         |                   |             |  |  |  |  |  |  |
| Course   | Objectives:  |          |         |                   |             |  |  |  |  |  |  |
| 1. To e  | xpose students to basic concepts of computer organization                                  | l.       |         |                   |             |  |  |  |  |  |  |
| 2. To p  | rovide a comprehensive and self contained view of contro                                   | l unit o | lesign  | l <b>.</b>        |             |  |  |  |  |  |  |
| 3. To an   | alyze performance issues in processor and memory design of a                               | digital  | compi   | iter.             |             |  |  |  |  |  |  |
| 4. To le   | arn concepts of pipeline architectures and different perform                               | mance    | meas    | ures.             |             |  |  |  |  |  |  |
| 5. To u  | nderstand parallel and distributed memory architectures.                                   |          |         |                   |             |  |  |  |  |  |  |
| Course Learning Outcomes:  |  |          |         |                   |             |  |  |  |  |  |  |
| CO   | After the completion of the course the student should                                      | be       |         |                   |             |  |  |  |  |  |  |
|  | able to  |          |         |                   |             |  |  |  |  |  |  |
| CO1  | Explain the organization of basic computer and its function, in data formats               | nstructi | on typ  | es and            | L           |  |  |  |  |  |  |
| CO2  | Design a simple control unit for the given task by applying the                            | e theory | y conc  | epts.             |             |  |  |  |  |  |  |
| CO3  | Analyze some of the design issues in terms of speed, technology, cost, performance.        |          |         |                   |             |  |  |  |  |  |  |
| CO4  | Illustrate memory organization and memory management hardware.                             |          |         |                   |             |  |  |  |  |  |  |
| CO5  | Learn the concepts of parallel, pipelined and distributed computer architectures.          |          |         |                   |             |  |  |  |  |  |  |
| CO-PO Mapping:   |  |          |         |                   |             |  |  |  |  |  |  |

| CO         | PO | PSO | PSO |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|-----|-----|
|            | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 1   | 2   |
| CO1        | 2  |    |    |    |    |    |    |    |    |    |    |    |     |     |
| CO2        | 2  |    | 2  |    |    |    |    |    |    |    |    |    |     |     |
| <b>CO3</b> | 2  |    |    |    |    |    |    |    |    |    |    |    |     |     |
| <b>CO4</b> |    | 3  |    | 3  |    |    |    |    |    |    |    |    |     |     |
| CO5        |    | 2  |    |    |    |    |    |    |    |    |    |    |     |     |

#### Assessments :

## **Teacher Assessment:**

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weights respectively.

| Assessment | Marks |
|------------|-------|
| ISE 1      | 10    |
| MSE        | 30    |
| ISE 2      | 10    |
| ESE        | 50    |

| MSE: Assessment is based on 50% of course content (Normally first three modules)         SE: Assessment is based on 100% course content with60-70% weightage for course content (normally last three modules) course content with60-70% weightage for course content (normally last three modules) course content with60-70% weightage for course content (normally last three modules) course content with60-70% weightage for course content (normally last three modules) course content with60-70% weightage for course content (normally last three modules)         Course Contents:       7 Hrs.         Evolution of computers - Electronic computers-generations, VLSI era , CPU organization , user and supervisor modes, accumulator based CPU, System bus, types of instruction (zero, one, two and three address machines), RISC& CISC, definition, comparison and examples, Data representation: Fixed-Point Numbers, Floating Point Number-The IEEE 754 floating pointing numbers       6 Hrs.         Introduction, multi cycle operation, implementation methods, Hardwired control, design methods, state tables, GCD processor, Classical method, one hot method, Design example twos complement, multipler control, CPU control unit design       6 Hrs.         Unit 3: Interoorperanmed Control, control field encoding, encoding by function, multiple microinstruction formats.       9 Hrs.         Unit 4: Memory Organization       9 Hrs.         Types of memory, Memory systems, multi level, address translation, memory allocation, Caches, Associative memory, direct mapping, set associative admessing.       6 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processors.       7 Hrs.         Unit 6: Distributed Memory Architecture   | ISE 1 and ISE 2 are based on assignment/declared test/quiz/seminar/Group Discuss   |                                     |  |  |  |  |  |  |
|--|--|-------------------------------------|--|--|--|--|--|--|
| ESE: Assessment is based on 100% course content winh60-70% weightage for course content (normally last three modules) covered after MSE.       7 Hrs.         Course Contents:       7 Hrs.         Unit 1: Basic Computer Organization       7 Hrs.         Evolution of computers - Electronic computers-generations, VLSI era , CPU organization , user and supervisor modes, accumulator based CPU, System bus, types of instruction(zero, one, two and three address machines), RISC& CISC, definition, comparison and examples, Data representation: Fixed-Point Numbers, Floating Point Number- The IEEE 754 floating pointing numbers       6 Hrs.         Introduction, multi cycle operation, implementation methods, Hardwired control, design methods, state tables, GCD processor, Classical method, one hot method, Design example twos complement multiplier control, CPU control unit design       6 Hrs.         Basic concepts, control unit organization, parallelism in microinstructions, Microinstruction formats.       9 Hrs.         Unit 4: Memory Organization formats.       9 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processing       9 Hrs.         Types of memory, Memory systems, multi level, address translation, memory allocation, Caches, Associative memory, direct mapping, set associative admerssing       6 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processors       7 Hrs.         Unit 6:Distributed Memory Architecture       7 Hrs.         Lossification, Introduction to Associative memory processors.       7 Hrs.         1: Computer Architecture & Parallel Pr  | MSE: Assessment is based on 50% of course content (Normally first three modules  |                                     |  |  |  |  |  |  |
| (normally last three modules) covered after MSE.       Course Contents:         (This Basic Computer Organization<br>Evolution of computers - Electronic computers-generations, VLSI era , CPU<br>organization , user and supervisor modes, accumulator based CPU, System bus,<br>types of instruction(zero, one, two and three address machines), RISC& CISC,<br>definition, comparison and examples, Data representation: Fixed - Point Numbers,<br>Floating Point Number - The IEEE 754 floating pointing numbers       6 Hrs.         Unit 2: Hardwired Control Design<br>Introduction, multi cycle operation, implementation methods, Hardwired control,<br>design methods, state tables, GCD processor, Classical method, one hot method,<br>Design example twos complement multiplier control, CPU control unit design       6 Hrs.         Unit 3: Microprogrammed Control Design<br>Unit 3: Microprogrammed Control Control field encoding, encoding by<br>function, multiplier control, Control field encoding, encoding by<br>function, multiplier control, Control field encoding, encoding by<br>function, multiple microinstruction formats.       9 Hrs.         Unit 4: Memory Organization<br>Types of memory, Memory systems, multi level, address translation, memory<br>allocation, Caches, Associative memory, direct mapping, set associative<br>addressing       9 Hrs.         Unit 6:Distributed Memory Architecture<br>Lossely coupled and tightly coupled architectures. Cluster computing as an<br>application of losely coupled architecture. Examples – CM*.       7 Hrs.         Textbooks:       1. Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)<br>2. Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)<br>2. Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)<br>2. Computer Architecture & Parallel Processing – Kai Hwa   | ESE: Assessment is based on 100% course content with60-70% weightage for course conten |                                     |  |  |  |  |  |  |
| Course Contents:       7 Hrs.         Unit 1: Basic Computer Organization       7 Hrs.         Evolution of computers - Electronic computers-generations, VLSI era , CPU       organization , user and supervisor modes, accumulator based CPU, System bus, types of instruction(zero, one, two and three address machines), RISC& CISC, definition, comparison and examples, Data representation: Fixed-Point Numbers, Floating Point Number-The IEEE 754 floating pointing numbers       6 Hrs.         Unit 2: Hardwired Control Design       6 Hrs.         Introduction, multi cycle operation, implementation methods, Hardwired control, design methods, state tables, GCD processor, Classical method, one hot method, Design example twos complement multiplier control, CPU control unit design       6 Hrs.         Basic concepts, control unit organization, parallelism in microinstructions, Microinstruction addressing, timing, Control unit organization, Design example-twos complement, multiple control, Control field encoding, encoding by function, multiple microinstruction formats.       9 Hrs.         Unit 4: Memory Organization       9 Hrs.         Types of memory, Memory systems, multi level, address translation, memory allocation, Caches, Associative memory, direct mapping, set associative addressing       6 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processing       6 Hrs.         Toti 6: Distributed Memory Architecture       1 Associative memory processors.       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*. <td< td=""><td>(normally last three modules) covered after MSE.</td><td></td></td<>   | (normally last three modules) covered after MSE.   |                                     |  |  |  |  |  |  |
| Unit 1: Basic Computer Organization       7 Hrs.         Evolution of computers - Electronic computers-generations, VLSI era , CPU       organization , user and supervisor modes, accumulator based CPU, System bus, types of instruction(zero, one, two and three address machines), RISC& CISC, definition, comparison and examples, Data representation: Fixed - Point Numbers.       6 Hrs.         Floating Point Number- The IEEE 754 floating pointing numbers       6 Hrs.         Introduction, mult cycle operation, implementation methods, Hardwired control, design methods, state tables, GCD processor, Classical method, one hot method, Design example twos complement multiplier control, CPU control unit design       6 Hrs.         Basic concepts, control unit organization, parallelism in microinstructions, Microinstruction addressing, timing, Control mit organization, Design exampletwos complement, multiplier control, Control field encoding, encoding by function, multiple microinstruction formats.       9 Hrs.         Unit 4: Memory Organization       9 Hrs.         Types of memory, Memory systems, multi level, address translation, memory allocation, Caches, Associative memory, direct mapping, set associative addressing       6 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processing       6 Hrs.         Flynn's Classification, Introduction to Associative memory processors, Unit 6:Distributed Memory Architecture       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture Examples – CM*.       7 Hrs.         1. Computer Architecture and Organization   | Course Contents:   | 1                                   |  |  |  |  |  |  |
| Evolution of computers - Electronic computers-generations, VLSI era , CPU         organization , user and supervisor modes, accumulator based CPU, System bus, types of instruction(zero, one, two and three address machines), RISC& CISC, definition, comparison and examples, Data representation: Fixed - Point Numbers, Floating Point Number - The IEEE 754 floating pointing numbers         Unit 2: Hardwired Control Design       6 Hrs.         Introduction, multi cycle operation, implementation methods, Hardwired control, design example twos complement multiplier control, CPU control unit design       6 Hrs.         Unit 3: Microprogrammed Control Design       6 Hrs.         Basic concepts, control unit organization, parallelism in microinstructions, Microinstruction addressing, timing, Control unit organization, Design example-twos complement, multiplier control, Control field encoding, encoding by function, multiple microinstruction formats.       9 Hrs.         Unit 3: Introduction to Pipeline and Parallel Processing       6 Hrs.         Pipelning, linear pipelining, classification of pipeline processors.       6 Hrs.         Unit 6:Distributed Memory Architecture       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an application of losely coupled architecture - Kai Hwang & Briggs (MGH)       7 Hrs.         1. Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)       2 Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)         2. Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)       2 Computer Architecture & Paral  | Unit 1: Basic Computer Organization  | 7 Hrs.                              |  |  |  |  |  |  |
| organization , user and supervisor modes, accumulator based CPU, System bus,         types of instruction(zero, one, two and three address machines), RISC& CISC,         definition, comparison and examples, Data representation: Fixed - Point Numbers,         Floating Point Number- The IEEE 754 floating pointing numbers         Unit 2: Hardwired Control Design         Introduction, multi cycle operation, implementation methods, Hardwired control,         design methods, state tables, GCD processor, Classical method, one hot method,         Design example twos complement multiplier control, CPU control unit design         Unit 3: Microprogrammed Control Design         Basic concepts, control unit organization, parallelism in microinstructions,         Microinstruction addressing, timing, Control unit organization, Design example-         twos complement, multiplier control, Control field encoding, encoding by         function, multi organization         Types of memory, Memory systems, multi level, address translation, memory         aldressing         Unit 4: Memory Organization         Types of memory, Memory systems, multi level, address translation, memory         aldressification, Introduction to Associative memory processors.         Flynn's Classification, Introduction to Associative memory processors.         Unit 5: Distributed Memory Architecture         Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled arch  | Evolution of computers - Electronic computers-generations, VLSI era, CPU   |                                     |  |  |  |  |  |  |
| types of instruction(zero, one, two and three address machines), RISC& CISC, definition, comparison and examples, Data representation: Fixed - Point Numbers, Floating Point Number - The IEEE 754 floating pointing numbers       6 Hrs.         Unit 2: Hardwired Control Design       6 Hrs.         Introduction, multi cycle operation, implementation methods, Hardwired control, design methods, state tables, GCD processor, Classical method, one hot method, Design example twos complement multiplier control, CPU control unit design       6 Hrs.         Microinstruction addressing, timing, Control unit organization, Design example-twos complement, multiplier control, Control field encoding, encoding by function, multiple microinstruction formats.       9 Hrs.         Unit 4: Memory Organization       9 Hrs.         Types of memory, Memory systems, multi level, address translation, memory allocation, Caches, Associative memory, direct mapping, set associative addressing       6 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processing       6 Hrs.         Pipelining, linear pipelining, classification of pipeline processors.       7 Hrs.         Unit 6: Distributed Memory Architecture       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.       7 Hrs.         Textbooks:       1. Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition       2. Advanced computer architecture & Parallel Processing – Kai Hwang & Briggs (MGH)         2] Computer Architecture & Parallel Processing –   | organization, user and supervisor modes, accumulator based CPU, System bus,  |                                     |  |  |  |  |  |  |
| definition, comparison and examples, Data representation: Fixed - Point Numbers,       Floating Point Number - The IEEE 754 floating pointing numbers         Unit 2: Hardwired Control Design       6 Hrs.         Introduction, multi cycle operation, implementation methods, Hardwired control, design methods, state tables, GCD processor, Classical method, one hot method, Design example twos complement multiplier control, CPU control unit design       6 Hrs.         Unit 3: Microprogrammed Control Design       6 Hrs.         Basic concepts, control unit organization, parallelism in microinstructions, Microinstruction addressing, timing, Control field encoding, encoding by function, multiple microinstruction formats.       9 Hrs.         Vinit 4: Memory Organization       9 Hrs.         Types of memory, Memory systems, multi level, address translation, memory allocation, Caches, Associative memory, direct mapping, set associative addressing       6 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processing       6 Hrs.         Flynn's Classification, Introduction to Associative memory processors, Interleaved memory organizations, performance evaluation factors. Parallel Processors-Flynn's Classification, Introduction to Associative memory processors, Unit 6:Distributed Memory Architecture       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.       7 Hrs.         Textbooks:       1. Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH) 2] Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MG   | types of instruction(zero, one, two and three address machines), RISC& CISC,   |                                     |  |  |  |  |  |  |
| Floating Point Number - The IEEE /54 floating pointing numbers       6 Hrs.         Unit 2: Hardwired Control Design       6 Hrs.         Introduction, multi cycle operation, implementation methods, Hardwired control, design methods, state tables, GCD processor, Classical method, one hot method, Design example twos complement multiplier control, CPU control unit design       6 Hrs.         Basic concepts, control unit organization, parallelism in microinstructions, Microinstruction addressing, timing, Control unit organization, Design exampletwos complement, multiplier control, Control field encoding, encoding by function, multiple microinstruction formats.       9 Hrs.         Unit 4: Memory Organization       9 Hrs.         Types of memory, Memory systems, multi level, address translation, memory allocation, Caches, Associative memory, direct mapping, set associative addressing       6 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processing       9 Hrs.         Pipelining, linear pipelining, classification of pipeline processors.       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.       7 Hrs.         Textbooks:       1. Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)       2] Computer Organization - Hamacher Zaky (MGH).         2] Computer Organization - Hamacher Zaky (MGH).       2] Computer system.       3 Students will be able to differentiate between control unit design methods.         3 Students will be able to differentiate and evaluate   | definition, comparison and examples, Data representation: Fixed - Point Numbers,   |                                     |  |  |  |  |  |  |
| Unit 2: Hardwired Control Design       6 Hrs.         Introduction, multi cycle operation, implementation methods, Hardwired control, design methods, state tables, GCD processor, Classical method, one hot method, Design example twos complement multiplier control, CPU control unit design       6 Hrs.         Basic concepts, control unit organization, parallelism in microinstructions, Microinstruction addressing, timing, Control unit organization, Design example-twos complement, multiplier control, Control field encoding, encoding by function, multiple microinstruction formats.       9 Hrs.         Unit 4: Memory Organization       9 Hrs.         Types of memory, Memory systems, multi level, address translation, memory allocation, Caches, Associative memory, direct mapping, set associative addressing       6 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processing       6 Hrs.         Pipelining, linear pipelining, classification of pipeline processors Interleaved memory organization, Introduction to Associative memory processors, Unit 6:Distributed Memory Architecture       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.       7 Hrs.         I. Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)       2) Computer Organization - Hamacher Zaky (MGH).         2] Computer Organization - Hamacher Zaky (MGH).       31 Computer system.       2 Students will be able to understand the basic organization of computer system.         2] Students will be able to differentiate between control unit design method   | Floating Point Number- The IEEE 754 floating pointing numbers  |                                     |  |  |  |  |  |  |
| Introduction, multi cycle operation, implementation methods, Hardwired control,<br>design methods, state tables, GCD processor, Classical method, one hot method,<br>Design example twos complement multiplier control, CPU control unit design<br>Unit 3: Microprogrammed Control Design<br>Basic concepts, control unit organization, parallelism in microinstructions,<br>Microinstruction addressing, timing, Control unit organization, Design example-<br>twos complement, multiplier control, Control field encoding, encoding by<br>function, multiple microinstruction formats.<br>Unit 4: Memory Organization<br>Types of memory, Memory systems, multi level, address translation, memory<br>allocation, Caches, Associative memory, direct mapping, set associative<br>addressing<br>Unit 5: Introduction to Pipeline and Parallel Processing<br>Pipelining, linear pipelining, classification of pipeline processors Interleaved<br>memory organizations, performance evaluation factors. Parallel Processors-<br>Flynn's Classification, Introduction to Associative memory processors,<br>Unit 6:Distributed Memory Architecture<br>Loosely coupled and tightly coupled architectures. Cluster computing as an<br>application of loosely coupled architecture. Examples – CM*.<br><b>Textbooks:</b><br>1. Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition<br>2. Advanced computer architecture – Kai Hwang(MGH)<br><b>References:</b><br>1] Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)<br>2] Computer Organization - Hamacher Zaky (MGH).<br>2] Computer Organization - Hamacher Zaky (MGH).<br>3 Students will be able to understand the basic organization of computer system.<br>3 Students will be able to differentiate between control unit design methods.<br>3 Students will be able to differentiate and evaluate performance of various memory<br>levels.<br>5 Students will be able to explain various parallel processing architectures.<br>6 Students will be able to understand the distributed memory architectures. | Unit 2: Hardwired Control Design   | 6 Hrs.                              |  |  |  |  |  |  |
| design methods, state tables, GCD processor, Classical method, one hof method,         Design example twos complement multiplier control, CPU control unit design         Unit 3: Microprogrammed Control Design         Basic concepts, control unit organization, parallelism in microinstructions,         Microinstruction addressing, timing, Control unit organization, Design example-         twos complement, multiplier control, Control field encoding, encoding by         function, multiple microinstruction formats.         Unit 4: Memory Organization         Types of memory, Memory systems, multi level, address translation, memory         aldcessing         Unit 5: Introduction to Pipeline and Parallel Processing         Pipelining, linear pipelining, classification of pipeline processors.         Ivinit 6:Distributed Memory Architecture         Loosely coupled and tightly coupled architectures. Cluster computing as an application of losely coupled architecture. Examples – CM*.         Textbooks:         1. Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)         2] Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)         2] Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)         2] Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)         2] Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)         2] Computer Architecture & Parallel Processing – Kai Hwang & Briggs (M  | Introduction, multi cycle operation, implementation methods, Hardwired control,  |                                     |  |  |  |  |  |  |
| Design example twos complement multiplier control, CPU control unit design       6 Hrs.         Unit 3: Microprogrammed Control Design       6 Hrs.         Basic concepts, control unit organization, parallelism in microinstructions, Microinstruction addressing, timing, Control unit organization, Design example-twos complement, multiplier control, Control field encoding, encoding by function, multiple microinstruction formats.       9 Hrs.         Unit 4: Memory Organization       9 Hrs.         Types of memory, Memory systems, multi level, address translation, memory allocation, Caches, Associative memory, direct mapping, set associative addressing       6 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processing       6 Hrs.         Pipelining, linear pipelining, classification of pipeline processors.       7 Hrs.         Unit 6:Distributed Memory Architecture       7 Hrs.         Lossely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.       7 Hrs.         Textbooks:       1. Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition 2. Advanced computer architecture – Kai Hwang(MGH).       2         Unit wise Measurable students Learning Outcomes:       1 Students will be able to understand the basic organization of computer system.         2 Students will be able to differentiate between control unit design methods.       3 Students will be able to differentiate and evaluate performance of various memory levels.         5 Students will be able to explain   | design methods, state tables, GCD processor, Classical method, one hot method,   |                                     |  |  |  |  |  |  |
| Unit 3: Microprogrammed Control Design       6 Hrs.         Basic concepts, control unit organization, parallelism in microinstructions,<br>Microinstruction addressing, timing, Control unit organization, Design example-<br>twos complement, multiplier control, Control field encoding, encoding by<br>function, multiple microinstruction formats.       9 Hrs.         Unit 4: Memory Organization       9 Hrs.         Types of memory, Memory systems, multi level, address translation, memory<br>allocation, Caches, Associative memory, direct mapping, set associative<br>addressing       6 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processing<br>Pipelining, linear pipelining, classification of pipeline processors Interleaved<br>memory organizations, performance evaluation factors. Parallel Processors-<br>Flynn's Classification, Introduction to Associative memory processors,       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an<br>application of loosely coupled architecture. Examples – CM*.       7 Hrs.         References:<br>1] Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition<br>2. Advanced computer architecture – Kai Hwang(MGH)       7         II Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)<br>2] Computer Organization - Hamacher Zaky (MGH).       1         Unit wise Measurable students Learning Outcomes:<br>1 Students will be able to understand the basic organization of computer system.       2         Students will be able to differentiate between control unit design methods.<br>3 Students will be able to differentiate and evaluate performance of various memory <b< td=""><td>Design example twos complement multiplier control, CPU control unit design</td><td></td></b<>   | Design example twos complement multiplier control, CPU control unit design   |                                     |  |  |  |  |  |  |
| Basic concepts, control unit organization, parallelism in microinstructions,<br>Microinstruction addressing, timing, Control unit organization, Design example-<br>twos complement, multiplier control, Control field encoding, encoding by<br>function, multiple microinstruction formats.       9 Hrs.         Unit 4: Memory Organization<br>Types of memory, Memory systems, multi level, address translation, memory<br>allocation, Caches, Associative memory, direct mapping, set associative<br>addressing       9 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processing<br>Pipelining, linear pipelining, classification of pipeline processors.       6 Hrs.         Pipelining, linear pipelining, classification of pipeline processors,<br>Flynn's Classification, Introduction to Associative memory processors,<br>Flynn's Classification, Introduction to Associative memory processors,<br>Unit 6:Distributed Memory Architecture<br>Loosely coupled and tightly coupled architectures. Cluster computing as an<br>application of loosely coupled architecture. Examples – CM*.       7 Hrs.         Textbooks:<br>1. Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition<br>2. Advanced computer architecture – Kai Hwang(MGH)       7         Unit wise Measurable students Learning Outcomes:<br>1 Students will be able to differentiate between control unit design methods.<br>3 Students will be able to differentiate between control unit design methods.<br>3 Students will be able to differentiate and evaluate performance of various memory<br>levels.         5 Students will be able to explain various parallel processing architectures.<br>6 Students will be able to understand the distributed memory architectures.   | Unit 3: Microprogrammed Control Design   | 6 Hrs.                              |  |  |  |  |  |  |
| Microinstruction addressing, timing, Control unit organization, Design example-<br>twos complement, multiplier control, Control field encoding, encoding by<br>function, multiple microinstruction formats.       9 Hrs.         Unit 4: Memory Organization       9 Hrs.         Types of memory, Memory systems, multi level, address translation, memory<br>allocation, Caches, Associative memory, direct mapping, set associative<br>addressing       6 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processing       6 Hrs.         Pipelining, linear pipelining, classification of pipeline processors Interleaved<br>memory organizations, performance evaluation factors. Parallel Processors-<br>Flynn's Classification, Introduction to Associative memory processors.       7 Hrs.         Unit 6:Distributed Memory Architecture       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an<br>application of loosely coupled architecture. Examples – CM*.       7 Hrs.         Textbooks:       1. Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition<br>2. Advanced computer architecture – Kai Hwang(MGH)         2] Computer Organization - Hamacher Zaky (MGH).       2]<br>Unit wise Measurable students Learning Outcomes:<br>1 Students will be able to understand the basic organization of computer system.         2 Students will be able to differentiate between control unit design methods.<br>3 Students will be able to differentiate and evaluate performance of various memory<br>levels.         5 Students will be able to explain various parallel processing architectures.<br>5 Students will be able to understand the distributed memory architectures.  | Basic concepts, control unit organization, parallelism in microinstructions,   |                                     |  |  |  |  |  |  |
| twos complement, multiplier control, Control field encoding, encoding by         function, multiple microinstruction formats.       9 Hrs.         Unit 4: Memory Organization       9 Hrs.         Types of memory, Memory systems, multi level, address translation, memory       6 Hrs.         glocation, Caches, Associative memory, direct mapping, set associative       6 Hrs.         Pipelining, linear pipelining, classification of pipeline processors Interleaved       6 Hrs.         Flynn's Classification, Introduction to Associative memory processors.       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.       7 Hrs.         Textbooks:       1. Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition       2. Advanced computer architecture - Kai Hwang & Briggs (MGH)         2] Computer Organization - Hamacher Zaky (MGH).       12 Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)       2] Computer Organization - Hamacher Zaky (MGH).         Unit wise Measurable students Learning Outcomes:       1 Students will be able to understand the basic organization of computer system.       2 Students will be able to differentiate between control unit design methods.         3 Students will be able to differentiate and evaluate performance of various memory levels.       5 Students will be able to explain various parallel processing architectures.         6 Students will be able to understand the distributed memory architectures  | Microinstruction addressing, timing, Control unit organization, Design example-  |                                     |  |  |  |  |  |  |
| tunction, multiple microinstruction formats.       9 Hrs.         Unit 4: Memory Organization       9 Hrs.         Types of memory, Memory systems, multi level, address translation, memory allocation, Caches, Associative memory, direct mapping, set associative addressing       6 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processing       6 Hrs.         Pipelining, linear pipelining, classification of pipeline processors Interleaved memory organizations, performance evaluation factors. Parallel Processors-Flynn's Classification, Introduction to Associative memory processors,       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.       7 Hrs.         Textbooks:       1. Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition       2. Advanced computer architecture – Kai Hwang(MGH)         Vinit wise Measurable students Learning Outcomes:       1       Students will be able to understand the basic organization of computer system.         2 Students will be able to differentiate between control unit design methods.       3       3         3 Students will be able to differentiate and evaluate performance of various memory levels.       5       5         5 Students will be able to explain various parallel processing architectures.       6       6   | twos complement, multiplier control, Control field encoding, encoding by   |                                     |  |  |  |  |  |  |
| Unit 4: Memory Organization       9 Hrs.         Types of memory, Memory systems, multi level, address translation, memory allocation, Caches, Associative memory, direct mapping, set associative addressing       9 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processing       6 Hrs.         Pipelining, linear pipelining, classification of pipeline processors Interleaved memory organizations, performance evaluation factors. Parallel Processors-Flynn's Classification, Introduction to Associative memory processors,       6 Hrs.         Unit 6:Distributed Memory Architecture       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.       7 Hrs.         Textbooks:       1. Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition 2. Advanced computer architecture – Kai Hwang(MGH)       7         I Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH) 2] Computer Organization - Hamacher Zaky (MGH).       2         Unit wise Measurable students Learning Outcomes:       1         1 Students will be able to understand the basic organization of computer system.       2         2 Students will be able to differentiate and evaluate performance of various memory levels.       5         5 Students will be able to explain various parallel processing architectures.       6         6 Students will be able to understand the distributed memory architectures.       6   | function, multiple microinstruction formats.   |                                     |  |  |  |  |  |  |
| Types of memory, Memory systems, multi level, address translation, memory allocation, Caches, Associative memory, direct mapping, set associative addressing       6 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processing       6 Hrs.         Pipelining, linear pipelining, classification of pipeline processors Interleaved memory organizations, performance evaluation factors. Parallel Processors-Flynn's Classification, Introduction to Associative memory processors,       7 Hrs.         Unit 6:Distributed Memory Architecture       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.       7 Hrs.         Textbooks:       1. Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition       2. Advanced computer architecture – Kai Hwang(MGH)         2] Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)       2] Computer Organization - Hamacher Zaky (MGH).         Unit wise Measurable students Learning Outcomes:       1 Students will be able to understand the basic organization of computer system.         2 Students will be able to differentiate between control unit design methods.       3 Students will be able to differentiate and evaluate performance of various memory levels.         5 Students will be able to explain various parallel processing architectures.       6 Students will be able to understand the distributed memory architectures.   | Unit 4: Memory Organization  | 9 Hrs.                              |  |  |  |  |  |  |
| allocation, Caches, Associative memory, direct mapping, set associative addressing       6 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processing       6 Hrs.         Pipelining, linear pipelining, classification of pipeline processors Interleaved memory organizations, performance evaluation factors. Parallel Processors-Flynn's Classification, Introduction to Associative memory processors,       6 Hrs.         Unit 6:Distributed Memory Architecture       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.       7 Hrs.         Textbooks:       1. Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition       2. Advanced computer architecture – Kai Hwang(MGH)         2] Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)       2] Computer Organization - Hamacher Zaky (MGH).         Unit wise Measurable students Learning Outcomes:       1       Students will be able to differentiate between control unit design methods.         3 Students will be able to differentiate and evaluate performance of various memory levels.       5       Students will be able to explain various parallel processing architectures.         6 Students will be able to understand the distributed memory architectures.       6       Students will be able to understand the distributed memory architectures.  | Types of memory, Memory systems, multi level, address translation, memory  |                                     |  |  |  |  |  |  |
| addressing       6 Hrs.         Unit 5: Introduction to Pipeline and Parallel Processing       6 Hrs.         Pipelining, linear pipelining, classification of pipeline processors Interleaved       6 Hrs.         Pipelining, linear pipelining, classification of pipeline processors Interleaved       6 Hrs.         Pipelining, linear pipelining, classification of pipeline processors Interleaved       6 Hrs.         Pipelining, linear pipelining, classification of pipeline processors.       7 Hrs.         Unit 6:Distributed Memory Architecture       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.       7 Hrs.         Textbooks:       1. Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition       2. Advanced computer architecture – Kai Hwang(MGH)         2. Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)       2] Computer Organization - Hamacher Zaky (MGH).         Unit wise Measurable students Learning Outcomes:       1       Students will be able to differentiate between control unit design methods.         3 Students will be able to differentiate and evaluate performance of various memory levels.       5         5 Students will be able to explain various parallel processing architectures.       6         6 Students will be able to understand the distributed memory architectures.       6  | allocation, Caches, Associative memory, direct mapping, set associative  |                                     |  |  |  |  |  |  |
| Unit S: Introduction to Pipeline and Parallel Processing       6 Hrs.         Pipelining, linear pipelining, classification of pipeline processors Interleaved       7 Hrs.         Pipelining, linear pipelining, classification of pipeline processors.       7 Hrs.         Unit 6:Distributed Memory Architecture       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.       7 Hrs.         Textbooks:       1. Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition       2. Advanced computer architecture – Kai Hwang(MGH)         I Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)       2] Computer Organization - Hamacher Zaky (MGH).         Unit wise Measurable students Learning Outcomes:       1 Students will be able to understand the basic organization of computer system.         2 Students will be able to differentiate between control unit design methods.       3 Students will be able to differentiate and evaluate performance of various memory levels.         5 Students will be able to explain various parallel processing architectures.       6 Students will be able to understand the distributed memory architectures.  | addragging   |                                     |  |  |  |  |  |  |
| Pipelining, linear pipelining, classification of pipeline processors Interleaved memory organizations, performance evaluation factors. Parallel Processors-Flynn's Classification, Introduction to Associative memory processors, <b>Unit 6:Distributed Memory Architecture 7 Hrs.</b> Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*. <b>7 Hrs. Textbooks:</b> 1. Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition       2. Advanced computer architecture – Kai Hwang(MGH) <b>References:</b> 1] Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)       2] Computer Organization - Hamacher Zaky (MGH). <b>Unit wise Measurable students Learning Outcomes:</b> 1 Students will be able to understand the basic organization of computer system.         2 Students will be able to differentiate between control unit design methods.       3 Students will be able to differentiate and evaluate performance of various memory levels.         5 Students will be able to explain various parallel processing architectures.       6 Students will be able to understand the distributed memory architectures.  |  |                                     |  |  |  |  |  |  |
| memory organizations, performance evaluation factors. Parallel Processors-<br>Flynn's Classification, Introduction to Associative memory processors,       7 Hrs.         Unit 6:Distributed Memory Architecture<br>Loosely coupled and tightly coupled architectures. Cluster computing as an<br>application of loosely coupled architecture. Examples – CM*.       7 Hrs.         Textbooks:       1. Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition       2. Advanced computer architecture – Kai Hwang(MGH)         References:       1] Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)       2] Computer Organization - Hamacher Zaky (MGH).         Unit wise Measurable students Learning Outcomes:       1 Students will be able to understand the basic organization of computer system.         2 Students will be able to differentiate between control unit design methods.       3 Students will be able to differentiate and evaluate performance of various memory<br>levels.         5 Students will be able to explain various parallel processing architectures.       6 Students will be able to understand the distributed memory architectures.  | Unit 5: Introduction to Pipeline and Parallel Processing   | 6 Hrs.                              |  |  |  |  |  |  |
| Flynn's Classification, Introduction to Associative memory processors,       7 Hrs.         Unit 6:Distributed Memory Architecture       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.       7 Hrs.         Textbooks:       1. Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition       2. Advanced computer architecture – Kai Hwang(MGH)         References:       1. Computer Architecture & Parallel Processing – Kai Hwang & Briggs (MGH)       2. Computer Organization - Hamacher Zaky (MGH).         Unit wise Measurable students Learning Outcomes:       1 Students will be able to understand the basic organization of computer system.         2 Students will be able to differentiate between control unit design methods.       3 Students will be able to differentiate and evaluate performance of various memory levels.         5 Students will be able to explain various parallel processing architectures.       6 Students will be able to understand the distributed memory architectures.  | Unit 5: Introduction to Pipeline and Parallel Processing<br>Pipelining, linear pipelining, classification of pipeline processors Interleaved   | 6 Hrs.                              |  |  |  |  |  |  |
| Unit 6:Distributed Memory Architecture       7 Hrs.         Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.       7         Textbooks:       1. Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition       2. Advanced computer architecture – Kai Hwang(MGH)         2. Advanced computer architecture & Parallel Processing – Kai Hwang & Briggs (MGH)       2] Computer Organization - Hamacher Zaky (MGH).         Vinit wise Measurable students Learning Outcomes:       1         1 Students will be able to understand the basic organization of computer system.         2 Students will be able to differentiate between control unit design methods.         3 Students will be able to differentiate and evaluate performance of various memory levels.         5 Students will be able to explain various parallel processing architectures.         6 Students will be able to understand the distributed memory architectures.   | Unit 5: Introduction to Pipeline and Parallel Processing<br>Pipelining, linear pipelining, classification of pipeline processors Interleaved<br>memory organizations, performance evaluation factors. Parallel Processors-   | 6 Hrs.                              |  |  |  |  |  |  |
| <ul> <li>Loosely coupled and ughtly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.</li> <li><b>Textbooks:</b> <ol> <li>Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition</li> <li>Advanced computer architecture – Kai Hwang(MGH)</li> </ol> </li> <li><b>References:</b> <ol> <li>Computer Architecture &amp; Parallel Processing – Kai Hwang &amp; Briggs (MGH)</li> <li>Computer Organization - Hamacher Zaky (MGH).</li> </ol> </li> <li><b>Unit wise Measurable students Learning Outcomes:</b> <ol> <li>Students will be able to understand the basic organization of computer system.</li> <li>Students will be able to differentiate between control unit design methods.</li> <li>Students will be able to differentiate and evaluate performance of various memory levels.</li> <li>Students will be able to explain various parallel processing architectures.</li> </ol> </li> </ul>  | Unit 5: Introduction to Pipeline and Parallel Processing<br>Pipelining, linear pipelining, classification of pipeline processors Interleaved<br>memory organizations, performance evaluation factors. Parallel Processors-<br>Flynn's Classification, Introduction to Associative memory processors,   | 6 Hrs.                              |  |  |  |  |  |  |
| <ul> <li>Textbooks: <ol> <li>Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition</li> <li>Advanced computer architecture – Kai Hwang(MGH)</li> </ol> </li> <li>References: <ol> <li>Computer Architecture &amp; Parallel Processing – Kai Hwang &amp; Briggs (MGH)</li> <li>Computer Organization - Hamacher Zaky (MGH).</li> </ol> </li> <li>Unit wise Measurable students Learning Outcomes: <ol> <li>Students will be able to understand the basic organization of computer system.</li> <li>Students will be able to differentiate between control unit design methods.</li> <li>Students will be able to differentiate and evaluate performance of various memory levels.</li> <li>Students will be able to explain various parallel processing architectures.</li> </ol> </li> </ul>   | Unit 5: Introduction to Pipeline and Parallel ProcessingPipelining, linear pipelining, classification of pipeline processors Interleavedmemory organizations, performance evaluation factors. Parallel Processors-Flynn's Classification, Introduction to Associative memory processors,Unit 6:Distributed Memory Architecture   | 6 Hrs.<br>7 Hrs.                    |  |  |  |  |  |  |
| <ul> <li>1. Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition</li> <li>2. Advanced computer architecture – Kai Hwang(MGH)</li> <li>References: <ol> <li>Computer Architecture &amp; Parallel Processing – Kai Hwang &amp; Briggs (MGH)</li> <li>Computer Organization - Hamacher Zaky (MGH).</li> </ol> </li> <li>Unit wise Measurable students Learning Outcomes: <ol> <li>Students will be able to understand the basic organization of computer system.</li> <li>Students will be able to differentiate between control unit design methods.</li> <li>Students will be able to describe function of microprogrammed control unit.</li> <li>Students will be able to differentiate and evaluate performance of various memory levels.</li> <li>Students will be able to explain various parallel processing architectures.</li> <li>Students will be able to understand the distributed memory architectures.</li> </ol> </li> </ul>   | Unit 5: Introduction to Pipeline and Parallel ProcessingPipelining, linear pipelining, classification of pipeline processors Interleavedmemory organizations, performance evaluation factors. Parallel Processors-Flynn's Classification, Introduction to Associative memory processors,Unit 6:Distributed Memory ArchitectureLoosely coupled and tightly coupled architectures. Cluster computing as an   | 6 Hrs.<br>7 Hrs.                    |  |  |  |  |  |  |
| <ol> <li>Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition</li> <li>Advanced computer architecture – Kai Hwang(MGH)</li> <li>References:         <ol> <li>Computer Architecture &amp; Parallel Processing – Kai Hwang &amp; Briggs (MGH)</li> <li>Computer Organization - Hamacher Zaky (MGH).</li> </ol> </li> <li>Unit wise Measurable students Learning Outcomes:         <ol> <li>Students will be able to understand the basic organization of computer system.</li> <li>Students will be able to differentiate between control unit design methods.</li> <li>Students will be able to describe function of microprogrammed control unit.</li> <li>Students will be able to differentiate and evaluate performance of various memory levels.</li> <li>Students will be able to explain various parallel processing architectures.</li> <li>Students will be able to understand the distributed memory architectures.</li> </ol> </li> </ol>   | Unit 5: Introduction to Pipeline and Parallel ProcessingPipelining, linear pipelining, classification of pipeline processors Interleavedmemory organizations, performance evaluation factors. Parallel Processors-Flynn's Classification, Introduction to Associative memory processors,Unit 6:Distributed Memory ArchitectureLoosely coupled and tightly coupled architectures. Cluster computing as anapplication of loosely coupled architecture. Examples – CM*.   | 6 Hrs.<br>7 Hrs.                    |  |  |  |  |  |  |
| <ul> <li>2. Advanced computer architecture – Kai Hwang(MGH)</li> <li>References: <ol> <li>Computer Architecture &amp; Parallel Processing – Kai Hwang &amp; Briggs (MGH)</li> <li>Computer Organization - Hamacher Zaky (MGH).</li> </ol> </li> <li>Unit wise Measurable students Learning Outcomes: <ol> <li>Students will be able to understand the basic organization of computer system.</li> <li>Students will be able to differentiate between control unit design methods.</li> <li>Students will be able to describe function of microprogrammed control unit.</li> <li>Students will be able to differentiate and evaluate performance of various memory levels.</li> <li>Students will be able to explain various parallel processing architectures.</li> <li>Students will be able to understand the distributed memory architectures.</li> </ol> </li> </ul>   | Unit 5: Introduction to Pipeline and Parallel ProcessingPipelining, linear pipelining, classification of pipeline processors Interleavedmemory organizations, performance evaluation factors. Parallel Processors-Flynn's Classification, Introduction to Associative memory processors,Unit 6:Distributed Memory ArchitectureLoosely coupled and tightly coupled architectures. Cluster computing as anapplication of loosely coupled architecture. Examples – CM*.Textbooks:   | 6 Hrs.<br>7 Hrs.                    |  |  |  |  |  |  |
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| <ul> <li>levels.</li> <li>5 Students will be able to explain various parallel processing architectures.</li> <li>6 Students will be able to understand the distributed memory architectures.</li> </ul>  | <ul> <li>Unit 5: Introduction to Pipeline and Parallel Processing</li> <li>Pipelining, linear pipelining, classification of pipeline processors Interleaved memory organizations, performance evaluation factors. Parallel Processors-Flynn's Classification, Introduction to Associative memory processors,</li> <li>Unit 6:Distributed Memory Architecture</li> <li>Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.</li> <li>Textbooks: <ol> <li>Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition</li> <li>Advanced computer architecture – Kai Hwang(MGH)</li> </ol> </li> <li>References: <ol> <li>Computer Architecture &amp; Parallel Processing – Kai Hwang &amp; Briggs (MGH)</li> <li>Computer Organization - Hamacher Zaky (MGH).</li> </ol> </li> <li>Unit wise Measurable students Learning Outcomes: <ol> <li>Students will be able to understand the basic organization of computer system.</li> <li>Students will be able to differentiate between control unit design methods.</li> <li>Students will be able to describe function of microprogrammed control unit.</li> </ol> </li> </ul>  | 6 Hrs.<br>7 Hrs.                    |  |  |  |  |  |  |
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| 6 Students will be able to understand the distributed memory architectures.  | <ul> <li>Unit 5: Introduction to Pipeline and Parallel Processing</li> <li>Pipelining, linear pipelining, classification of pipeline processors Interleaved memory organizations, performance evaluation factors. Parallel Processors-Flynn's Classification, Introduction to Associative memory processors,</li> <li>Unit 6:Distributed Memory Architecture</li> <li>Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.</li> <li>Textbooks: <ol> <li>Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition</li> <li>Advanced computer architecture – Kai Hwang(MGH)</li> </ol> </li> <li>References: <ol> <li>Computer Architecture &amp; Parallel Processing – Kai Hwang &amp; Briggs (MGH)</li> <li>Computer Organization - Hamacher Zaky (MGH).</li> </ol> </li> <li>Unit wise Measurable students Learning Outcomes: <ol> <li>Students will be able to understand the basic organization of computer system.</li> <li>Students will be able to differentiate between control unit design methods.</li> <li>Students will be able to differentiate and evaluate performance of various memory levels.</li> </ol> </li> </ul>  | 6 Hrs.<br>7 Hrs.                    |  |  |  |  |  |  |
|  | <ul> <li>Unit 5: Introduction to Pipeline and Parallel Processing</li> <li>Pipelining, linear pipelining, classification of pipeline processors Interleaved memory organizations, performance evaluation factors. Parallel Processors-Flynn's Classification, Introduction to Associative memory processors,</li> <li>Unit 6:Distributed Memory Architecture</li> <li>Loosely coupled and tightly coupled architectures. Cluster computing as an application of loosely coupled architecture. Examples – CM*.</li> <li>Textbooks: <ol> <li>Computer Architecture and Organization - John P Hayes (MGH) 3rd Edition</li> <li>Advanced computer architecture – Kai Hwang(MGH)</li> </ol> </li> <li>References: <ol> <li>Computer Architecture &amp; Parallel Processing – Kai Hwang &amp; Briggs (MGH)</li> <li>Computer Organization - Hamacher Zaky (MGH).</li> </ol> </li> <li>Unit wise Measurable students Learning Outcomes: <ol> <li>Students will be able to differentiate between control unit design methods.</li> <li>Students will be able to differentiate and evaluate performance of various memor levels.</li> <li>Students will be able to explain various parallel processing architectures.</li> </ol> </li> </ul>  | <b>6 Hrs.</b><br><b>7 Hrs.</b><br>у |  |  |  |  |  |  |

| Title of  | f the Course: Software Engineering                            | L        | Т       | Р        | Credit |  |  |  |  |  |  |  |
|---|---|----------|---------|----------|--------|--|--|--|--|--|--|--|
| Course  | ourse Code: UCSE0405 3 3                                      |          |         |          |        |  |  |  |  |  |  |  |
| Course  | Course Pre-Requisite:   |          |         |          |        |  |  |  |  |  |  |  |
| -   |   |          |         |          |        |  |  |  |  |  |  |  |
| Course Description: This course provides basic concepts, principles of software engineering & |   |          |         |          |        |  |  |  |  |  |  |  |
| basics o  | basics of Project Management.                                 |          |         |          |        |  |  |  |  |  |  |  |
| Course  | e Objectives:   |          |         |          |        |  |  |  |  |  |  |  |
| 1. To ex  | pose the students to basic concepts, principles of software e | enginee  | ring &  | importa  | nce of |  |  |  |  |  |  |  |
| SDL   | C in their project development work.                          |          |         |          |        |  |  |  |  |  |  |  |
| 2. To ex  | pose the students to software testing techniques and softwa   | re quali | ty man  | agement  | *•     |  |  |  |  |  |  |  |
| 3. To in  | troduce students basics of Object Oriented Modeling and D     | esign.   |         |          |        |  |  |  |  |  |  |  |
| 4. To m   | ake the student aware of role of Software Engineering in Pr   | oject N  | lanagei | nent.    |        |  |  |  |  |  |  |  |
| C   | I   |          |         |          |        |  |  |  |  |  |  |  |
| Course  | e Learning Outcomes:  |          |         |          |        |  |  |  |  |  |  |  |
| CO  | After the completion of the course the student show           | ld ha    |         |          |        |  |  |  |  |  |  |  |
| CO  | After the completion of the course the student show           | ina be   |         |          |        |  |  |  |  |  |  |  |
| 001   | able to   |          |         |          |        |  |  |  |  |  |  |  |
| COI   | Explain the Software Development Process.                     |          |         | 1        |        |  |  |  |  |  |  |  |
| <b>CO2</b>  | Illustrate the Software Testing techniques and Quality        | y Assui  | rancei  | n detail |        |  |  |  |  |  |  |  |
| <b>CO3</b>  | Make use of Project management Concepts in the pro-           | ject de  | velop   | nent.    |        |  |  |  |  |  |  |  |
| <b>CO4</b>  | Design the solution to the problems using Object C            | )rientec | d Mod   | elling w | ith    |  |  |  |  |  |  |  |
|   | UML.  |          |         |          |        |  |  |  |  |  |  |  |

#### Mapping of Course Outcomes with Program Outcomes and Program Specific Outcomes

| CO<br>s | PO<br>1 | <b>PO</b><br>2 | PO<br>3 | <b>PO</b><br>4 | PO<br>5 | <b>PO</b><br>6 | <b>PO</b><br>7 | PO<br>8 | PO<br>9 | P<br>O<br>10 | P<br>O<br>11 | P<br>0<br>12 | PSO<br>1 | PSO<br>2 |
|---------|---------|----------------|---------|----------------|---------|----------------|----------------|---------|---------|--------------|--------------|--------------|----------|----------|
| CO<br>1 | 3       |                |         |                |         |                |                |         |         |              |              | -            |          |          |
| CO<br>2 |         |                |         |                |         |                |                |         |         |              |              | -            |          |          |
| CO<br>3 |         |                |         |                |         |                |                |         | 2       |              | 3            | -            | 1        |          |
| CO<br>4 |         | 2              | 3       | 1              | 1       |                |                |         | 3       |              | 2            |              | 1        | 2        |

Assessments :

**Teacher Assessment:** 

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weights respectively.

| Assessment | Marks |
|------------|-------|
| ISE 1      | 10    |

| MSE   | 30                               |                   |  |  |  |  |  |  |  |  |
|---|----------------------------------|-------------------|--|--|--|--|--|--|--|--|
| ISE 2   | 10                               |                   |  |  |  |  |  |  |  |  |
| ESE   | 50                               |                   |  |  |  |  |  |  |  |  |
| ISE 1 and ISE 2 are based on assignment/declared test/quiz/seminar/Group Discussions etc. |                                  |                   |  |  |  |  |  |  |  |  |
| MSE: Assessment is based on 50% of course content (Normally first three modules)          |                                  |                   |  |  |  |  |  |  |  |  |
| ESE: Assessment is based on 100% course content with60-70% weightage for course content   |                                  |                   |  |  |  |  |  |  |  |  |
| (normally last three modules) covered after MSE.  |                                  |                   |  |  |  |  |  |  |  |  |
|   |                                  |                   |  |  |  |  |  |  |  |  |
|   |                                  |                   |  |  |  |  |  |  |  |  |
| Course Contents:  |                                  |                   |  |  |  |  |  |  |  |  |
| Unit 1: The software Problem [Text Book-1   | 1                                | 5 Hrs.            |  |  |  |  |  |  |  |  |
| 1.1 Software Problems, Software Engineering   | g Problems                       | • • • • • • • • • |  |  |  |  |  |  |  |  |
| 1.2 Cost, schedule & Ouality, Scale and chan  | ge.                              |                   |  |  |  |  |  |  |  |  |
| 1.3 Software Development process Modules.   |                                  |                   |  |  |  |  |  |  |  |  |
| 1.4 Project Management Process  |                                  |                   |  |  |  |  |  |  |  |  |
| 1.5 Software Processes: Process & Project   |                                  |                   |  |  |  |  |  |  |  |  |
|   |                                  |                   |  |  |  |  |  |  |  |  |
| Unit 2: Requirements Analysis & specificati   | on_[Text Book-1,2]               | 6 Hrs.            |  |  |  |  |  |  |  |  |
| 2.1 Requirements gathering & Analysis   |                                  |                   |  |  |  |  |  |  |  |  |
| 2.2 Software Requirements Specifications  |                                  |                   |  |  |  |  |  |  |  |  |
| 2.3 Collecting Requirements, Defining Scope,  |                                  |                   |  |  |  |  |  |  |  |  |
| 2.4 Creating the Work Breakdown Structur  | e, Validating Scope, Controlling |                   |  |  |  |  |  |  |  |  |
| Scope   |                                  |                   |  |  |  |  |  |  |  |  |
| 2.5 Basic Principles of Cost Management,  |                                  |                   |  |  |  |  |  |  |  |  |
| 2.6 Planning Cost Management, Estimating Co   | osts,                            |                   |  |  |  |  |  |  |  |  |
| 2.7 Determining the Budget, Controlling Cos   | sts, Formal System Development   |                   |  |  |  |  |  |  |  |  |
| Techniques  |                                  |                   |  |  |  |  |  |  |  |  |
| Unit 3: Dosign [Toxt Book_1 2]  |                                  | 7 Hrs             |  |  |  |  |  |  |  |  |
| 3 1 Design Concepts   |                                  | / 11/5.           |  |  |  |  |  |  |  |  |
| 3.2 Function Oriented Design  |                                  |                   |  |  |  |  |  |  |  |  |
| 3.3 Object Oriented Design  |                                  |                   |  |  |  |  |  |  |  |  |
| 3 4 Detail Design   |                                  |                   |  |  |  |  |  |  |  |  |
| 3.5 Verification  |                                  |                   |  |  |  |  |  |  |  |  |
| 3.6 Metrics   |                                  |                   |  |  |  |  |  |  |  |  |
|   |                                  |                   |  |  |  |  |  |  |  |  |
| Unit 4: Object Oriented Modeling and Desig  | n [Text Book-3]                  | 6 Hrs.            |  |  |  |  |  |  |  |  |
| 4.1 Object Oriented Design : What is Object O   | rientation? What is OO           |                   |  |  |  |  |  |  |  |  |
| Development? OO Themes.   |                                  |                   |  |  |  |  |  |  |  |  |
| 4.2 Modeling as Design Techniques: Modeling   | g, Abstraction, Three Models     |                   |  |  |  |  |  |  |  |  |
| 4.3 Overview of UML [Text Book-4]   |                                  |                   |  |  |  |  |  |  |  |  |
| 4.4 Conceptual Model of UML   |                                  |                   |  |  |  |  |  |  |  |  |
| 4.5 Architecture  |                                  |                   |  |  |  |  |  |  |  |  |
|   |                                  |                   |  |  |  |  |  |  |  |  |
| Unit 5: Coding & Testing [Text Book-1]  |                                  | 7 <b>Hrs.</b>     |  |  |  |  |  |  |  |  |
| 4.1 Coding & Code Review  |                                  |                   |  |  |  |  |  |  |  |  |
| 4.2 Lesting   |                                  |                   |  |  |  |  |  |  |  |  |
| 4.5 Unit lesting  |                                  |                   |  |  |  |  |  |  |  |  |
| 4.4 DIACK DOX TESUNG  |                                  |                   |  |  |  |  |  |  |  |  |

| 4.5 White Box Testing                                       |        |
|---|--------|
| 4.6 Integration Testing                                     |        |
| 4.7 System Testing  |        |
|   |        |
| <u>Unit 6: Quality Management [Text Book-2,1]</u>           | 7 Hrs. |
| 5.1 Importance, Planning Quality Management,                |        |
| 5.2 Performing Quality Assurance, Controlling Quality,      |        |
| 5.3 Tools and Techniques for Quality Control,               |        |
| 5.4 Modern Quality Management, Improving IT Project Quality |        |
| 5.5 ISO 9000 SEI capability Maturity Model, Six Sigma       |        |
| 5.6 Agile software Development & Extreme Programming        |        |
| 5.7 Agile Project Management                                |        |
|   |        |

## **Textbooks:**

- 1. 1 Software Engineering : A precise Approach Pankaj Jalote (Wiley India)
- 2. Information Technology Project Management, 7E, Kathy Schwalbe, Cengage Learning (India Edition)
- 3. Object Oriented Modeling and Design with UML, Michel R Blaha, James R Rambaugh, Second Edition
- 4. The Unified Modelling Language User Guide: Grady Booch, James Rambaugh, Lvar Jacobson.

#### **References:**

- 1. IT Project Management, 3 E, Joseph Phillips, McGraw Hill Edu. (India) Pvt. Ltd.
- 2. Software Project Management, Bob Huges, Mike Cotterell, Rajib Mall, 5/E, Tata McGraw Hill Edu. (India) Pvt. Ltd.

#### Unit wise Measurable students Learning Outcomes:

After learning this unit the student will be able to-

- 1. Explain SDLC.
- 2. Explain software testing techniques and software quality management.
- 3. Illustrate basics of Object Oriented Modelling concepts.
- 4. Explain role of Quality in Project Management.

| Title of the Course: Object Oriented Progg. Using C++ Lab. | L | Т | Ρ | Cr |
|--|---|---|---|----|
| Course Code. OCSE0431                                      | 2 | 0 | 2 | 3  |

Course Prerequisite:

Knowledge of C programming

#### **Course Description:**

This course exposes students to the concepts of Object Oriented Programming (OOP). It helps students to choose proper OOP concepts to solve different problems. Upon completion, students should be able to write efficient, reusable programs for a given problem using OOP concepts.

#### **Course Learning Objectives:**

- 1. To expose the students to concepts of Object Oriented Paradigm.
- 2. To make students understand the use of programming constructs of C++.
- 3. To give hands on exposure to develop applications based on concepts of Object Oriented approach.

#### **Course Outcomes:**

| CO  | After the completion of the course the student should be able to                            |
|-----|---|
| CO1 | explain object oriented concepts, principles and techniques.                                |
| CO2 | select appropriate approach from procedural and object oriented to solve the given problem. |
| CO3 | apply various object oriented features to solve real life problems using C++ language.      |
| CO4 | make use of exception handling and STL to solve given problems.                             |

#### CO-PO Mapping:

| со  | PO<br>1 | PO<br>2 | PO<br>3 | РО<br>4 | PO<br>5 | PO<br>6 | РО<br>7 | PO<br>8 | РО<br>9 | PO<br>10 | PO<br>11 | PO<br>12 | PSO<br>1 | PSO<br>2 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|---------|----------|----------|----------|----------|----------|
| CO1 | 1       |         |         |         |         |         |         |         |         |          |          | 1        | 1        |          |
| CO2 | 2       | 1       |         |         |         |         |         |         |         |          |          | 1        |          |          |
| CO3 | 1       | 2       | 3       |         | 1       |         |         | 1       |         | 1        |          | 1        | 1        | 3        |
| CO4 | 1       | 2       | 2       |         | 2       |         |         | 1       |         |          |          | 1        | 1        | 2        |

#### Assessments :

#### **Teacher Assessment:**

One component of In Semester Evaluation (ISE) and one End Semester Examination (ESE) having 50%, and 50% weights respectively.

| Assessment | Marks |
|------------|-------|
| ISE        | 50    |
| ESE        | 50    |

ISE are based on practical performed/Quiz/Mini-Project assigned/Presentation/Group Discussion/Internal oral etc.

ESE: Assessment is based on practical and oral examination

#### **Course Contents:**

**Unit 1: Introduction:** Introduction to procedural & object-oriented programming, 03 **Hrs.** Limitations of procedural programming, Need of object-oriented programming,

| Fundamentals of object-oriented programming: objects, classes, data members,  |                 |
|---|-----------------|
| methods, messages, data encapsulation, data abstraction and information hiding,   |                 |
| inheritance, polymorphism.  |                 |
| Unit 2: Basics of C++ programming: Friend Functions, Friend Classes, Inline   | 04 Hrs.         |
| Functions, Parameterized constructors, Static class members, Scope resolution   |                 |
| operators, Passing objects to functions, nested classes, and local classes.   |                 |
| Unit 3: Inheritance: Need of Inheritance, Concept, public, private, protected   | 04 <b>Hrs.</b>  |
| inheritance, Single inheritance, Multiple and multilevel inheritance, Hybrid  |                 |
| Inheritance, Virtual base class, overriding of member functions, static variable,   |                 |
| static function, friend function, friend class  |                 |
| Unit 4: Polymorphism: Pointers basics of memory management, New and delete  | 06 <b>Hrs</b> . |
| operators, Pointer to object, Pointer to data members, this pointer. Need of  |                 |
| Polymorphism, concept, Compile time polymorphism or early binding: function   |                 |
| overloading and operator overloading, operator overloading using member   |                 |
| function and friend function, overloading - unary, binary, arithmetic operators,  |                 |
| relational operators, Overloading new and delete operators, insertion and   |                 |
| extraction operators, Run time polymorphism or late binding using Virtual function,   |                 |
| pure virtual function, Abstract class, Type conversion  |                 |
| Unit 5: Files and Streams: Concept of Streams, concept of File, opening and   | 05 <b>Hrs</b> . |
| closing a file, detecting end-of-file, file modes, file pointer, reading and writing  |                 |
| characters, strings and objects to the file, operations to move file pointers i.e   |                 |
| seekg, seekp, tellg, tellp.   |                 |
| Unit 6: Advanced C++ features: Introduction to Generic Programming using  | 06 <b>Hrs.</b>  |
| Templates: Function template and class template, Introduction to Standard   |                 |
| Template Library (STL), containers, iterators and algorithms, study of container  |                 |
| template classes for vectors and stacks and related algorithms 2 Exception  |                 |
| handling: Introduction, syntax for exception handling code: try-catch-throw,  |                 |
| Multiple Exceptions, Exceptions with arguments  |                 |
| Textbooks:  |                 |
| <ol> <li>C++ programming by Robert Lafore 4th Edition (SAMS)</li> </ol>   |                 |
| <ol><li>The Complete Reference: C++ - Herbert Schildt (TMGH) Fourth Edition.</li></ol>  |                 |
| References:   |                 |
| <ol> <li>C++ Programming with language - Bjarne Stroustrup, AT &amp; T</li> </ol>   |                 |
| 2. Object oriented Programming in C++ 3rd Edition-R.Lafore (Galgotia Publications)  |                 |
| 3. C++programming –John Thomas Berry(PHI) • Object –Oriented Analysis & Design:   |                 |
| Understanding System Development with UML 2.0, Docherty, Wiley India Ltd.   |                 |
| 4. http://www.spoken-tutorial.org/NMEICT Project of Govt. Of India.   |                 |
| Assignments & Laboratory Work:  |                 |
| Minimum 10-12 Experiments are to be performed in batches, on the above topi   | cs. Term        |
| work should comprise detailed documentation on the below 10-12 experiments.   | Students        |
| should implement programs based on the following topics preferably on Linux platfo  | orm.            |
| 1. Study of OOP features and compare it with POP.   |                 |
| 2. Functions with default (Optional) arguments.   |                 |
| 3. Classes (with constructor) and Objects.  |                 |
|   |                 |
| 4. Operator Overloading.  |                 |
| <ol> <li>4. Operator Overloading.</li> <li>5. Inheritance</li> </ol>  |                 |
| <ol> <li>4. Operator Overloading.</li> <li>5. Inheritance</li> <li>6. Memory Management</li> </ol>  |                 |
| <ul> <li>4. Operator Overloading.</li> <li>5. Inheritance</li> <li>6. Memory Management</li> <li>7. Polymorphism</li> </ul>   |                 |
| <ul> <li>4. Operator Overloading.</li> <li>5. Inheritance</li> <li>6. Memory Management</li> <li>7. Polymorphism</li> <li>8. Type Conversion</li> </ul>   |                 |
| <ul> <li>4. Operator Overloading.</li> <li>5. Inheritance</li> <li>6. Memory Management</li> <li>7. Polymorphism</li> <li>8. Type Conversion</li> <li>9. Exception Handling</li> </ul>  |                 |
| <ul> <li>4. Operator Overloading.</li> <li>5. Inheritance</li> <li>6. Memory Management</li> <li>7. Polymorphism</li> <li>8. Type Conversion</li> <li>9. Exception Handling</li> <li>10 Template</li> </ul>   |                 |
| <ul> <li>4. Operator Overloading.</li> <li>5. Inheritance</li> <li>6. Memory Management</li> <li>7. Polymorphism</li> <li>8. Type Conversion</li> <li>9. Exception Handling</li> <li>10. Template</li> <li>11 File Handling</li> </ul>                  |                 |
| <ul> <li>4. Operator Overloading.</li> <li>5. Inheritance</li> <li>6. Memory Management</li> <li>7. Polymorphism</li> <li>8. Type Conversion</li> <li>9. Exception Handling</li> <li>10. Template</li> <li>11. File Handling</li> <li>12 STL</li> </ul> |                 |

| Title of   | f the C  | ourse:   | Comp     | uter Gr  | aphics    | Lab      |          |         |          | ]       | LT        | P         | C      | redit |
|--|----------|----------|----------|----------|-----------|----------|----------|---------|----------|---------|-----------|-----------|--------|-------|
| Course Code: UCSE0432  |          |          |          |          |           |          |          |         |          |         | 2         |           | 1      |       |
| Course Pre-Requisite: C programming and mathematics                                      |          |          |          |          |           |          |          |         |          |         |           |           |        |       |
| Course Description: Study and implement basic and core techniques in Computer Graphics   |          |          |          |          |           |          |          |         |          |         |           |           |        |       |
| Course Objectives: To expose students to:-   |          |          |          |          |           |          |          |         |          |         |           |           |        |       |
| 1. Understand the need of developing graphics application                                |          |          |          |          |           |          |          |         |          |         |           |           |        |       |
| 2. Learn algorithmic development of graphics primitives like: line, circle, polygon etc. |          |          |          |          |           |          |          |         |          |         |           |           |        |       |
| 3. Learn the representation and transformation of graphical images and pictures.         |          |          |          |          |           |          |          |         |          |         |           |           |        |       |
| Course Learning Outcomes:  |          |          |          |          |           |          |          |         |          |         |           |           |        |       |
| CO After the completion of the course the student should be                              |          |          |          |          |           |          |          |         |          |         |           |           |        |       |
|  | able     | to       | <b>P</b> |          |           |          |          |         |          |         |           |           |        |       |
|  | Dev      | elop e   | effectiv | ve Op    | enGL      | prograi  | ns to    | solve   | graph    | ics pro | gramn     | ning iss  | sues,  |       |
| CO1  | inclu    | iding 3  | 3D tran  | sform    | ation, o  | bjects n | nodellir | ıg, col | our mo   | delling | , lightir | ıg, textı | ires,  |       |
|  | and      | ray tra  | cing.    |          |           | -        |          | -       |          | -       | -         | -         |        |       |
| CO2  | Mak      | e use    | of mo    | dern to  | ools suc  | ch as b  | lender,  | adobe   | e flash  | for dev | elopin    | g comp    | outer  |       |
| 02   | grap     | hics ap  | oplicat  | ions.    |           |          |          |         |          |         | Ĩ         | 0 1       |        |       |
| CO3  | Illus    | trate e  | ffects   | of vario | ous illui | minatio  | n mode   | els and | ray tra  | cing mo | ethods    | in comj   | outer  |       |
| 05   | grap     | hics.    |          |          |           |          |          |         |          |         |           |           |        |       |
|  | ) Mani   | nina     |          |          |           |          |          |         |          |         |           |           |        |       |
| 0-10   | Jurap    | ping.    |          |          |           |          |          |         |          |         |           |           |        |       |
| CO   | PO1      | PO2      | PO3      | PO4      | PO5       | PO6      | PO7      | PO8     | PO9      | PO10    | PO11      | PO12      | PSO1   | PSO2  |
| CO1  | 2        | 2        | 3        | 2        | 3         |          |          |         |          |         |           |           | 3      | 3     |
| CO2  | 2        | 2        | 3        | 2        | 3         |          |          |         |          |         |           |           | 3      | 3     |
|  | _        |          |          |          |           |          |          |         |          |         |           |           |        |       |
| CO3  | 2        | 2        | 3        | 2        | 3         |          |          |         |          |         |           |           | 3      | 3     |
| Assess   | nents :  |          |          |          |           |          |          |         |          |         |           |           |        |       |
| Teache   | er Asse  | ssment   | :        |          |           |          |          |         |          |         |           |           |        |       |
| One con  | mpone    | nts of I | n Seme   | ster Ev  | aluation  | (ISE) a  | nd one l | EndSer  | nester E | Examina | tion (ES  | SE) havi  | ng 50% | and   |
| 50% w  | eights r | respecti | ively.   |          |           |          |          |         |          |         |           |           |        |       |
| l  |          |          |          | ٦.4      | 1         |          |          |         |          |         | A         |           |        |       |

|                       | Marks  | Assessment ISE   |       |  |  |
|-----------------------|--|--|-------|--|--|
|                       | 25   |  |       |  |  |
|                       | 25   |  |       |  |  |
| Course Co             | ontents:   |  |       |  |  |
| Experime              | nt No. 1:- : OpenGL programming to use basic grap  | phics primitives   | 2 Hrs |  |  |
| Experime<br>transform | <b>nt No. 2:-</b> Write a menu driven program in C to imp<br>ation on two dimensional objects like rotation, refle | plement two dimensional ection, scaling and shearing using | 2 Hrs |  |  |

| Course Contents:  |       |
|---|-------|
| Experiment No. 1:-: OpenGL programming to use basic graphics primitives   | 2 Hrs |
| <b>Experiment No. 2:-</b> Write a menu driven program in C to implement two dimensional transformation on two dimensional objects like rotation, reflection, scaling and shearing using Open GL | 2 Hrs |

| <b>Experiment No. 3:-</b> Install the necessary packages in CentOS/Ubuntu for running the graphics program and include graphics.h header/libraries file in gcc compiler | 2 Hrs |
|---|-------|
| Experiment No.4:- Implementing Bresenham's line drawing algorithm.  | 2 Hrs |
| Experiment No. 5:- Implementing Bresenham's circle generation algorithm.  | 2 Hrs |
| Experiment No. 5:- Implementing Edge fill algorithm.  | 2 Hrs |
| Experiment No. 6:- Implementing Seed fill algorithm.  | 2 Hrs |
| Experiment No. 7:- Implementing Sutherland-Cohen line clipping algorithm.   | 2 Hrs |
| Experiment No. 8:- Implementing Basic Illumination Models   | 2 Hrs |
| Experiment No. 9:- Implementing Basic Ray Tracing algorithm.  | 2 Hrs |
| Textbooks:  |       |
| 1. Computer Graphics Using OpenGL F.S. Hill Jr. Stephen M. Kelley, (Pearson Education).   |       |
| Unit wise Measurable students Learning Outcomes:  |       |

| T:41 f     | the Commentary Networks Lab   | т       | т       | р        | Courd!4         |  |  |  |  |  |
|------------|---|---------|---------|----------|-----------------|--|--|--|--|--|
| Title of   | the Course: Computer Networks Lab   | L       | I       | P        | Creatt          |  |  |  |  |  |
| Course     | ourse Code: UCSE0433 2 1  |         |         |          |                 |  |  |  |  |  |
| Course     | Course Pre-Requisite: Data Communication and Networking Theory & Lab.                           |         |         |          |                 |  |  |  |  |  |
|            |   |         |         |          |                 |  |  |  |  |  |
| Course     | Description: Study top four layers of OSI networking model and                                  | nd imp  | lement  | exam     | ple programs at |  |  |  |  |  |
| differen   | at layers and use different networking tools.   |         |         |          |                 |  |  |  |  |  |
| Course     | Objectives: To expose students to:-   |         |         |          |                 |  |  |  |  |  |
| 1.         | Basic concepts of Client Server model of Internet using Socket prog                             | grammi  | ng      |          |                 |  |  |  |  |  |
| 2.         | Logical addressing of computers/nodes in LAN/WAN.   |         | -       |          |                 |  |  |  |  |  |
| 3.         | Application layer protocols such as HTTP, FTP, TELNET, DHCP e                                   | tc.     |         |          |                 |  |  |  |  |  |
| 4.         | Networking tools such as Packet Tracer TCPDUMP and Wireshark                                    | to anal | yze pro | otocols  |                 |  |  |  |  |  |
| Course     | Learning Outcomes:  |         |         |          |                 |  |  |  |  |  |
|            |   |         |         |          |                 |  |  |  |  |  |
| CO         | After the completion of the course the student should be  |         |         |          |                 |  |  |  |  |  |
|            | able to   |         |         |          |                 |  |  |  |  |  |
|            |   |         |         |          |                 |  |  |  |  |  |
| CO1        | Design network for an organization as per the requirements                                      |         |         |          |                 |  |  |  |  |  |
| CO2        | Design UDP and TCP client server program to demonstrate simple, iterative and concurrent server |         |         |          |                 |  |  |  |  |  |
| CO3        | Demonstrate working of different routing protocols and application                              | n layer | protoc  | cols usi | ing             |  |  |  |  |  |
|            | Wireshark/Packet Tracer/TCPDump   | -       | •       |          | -               |  |  |  |  |  |
| <b>CO4</b> | Design client client server program to send and receive email, web                              | pages.  |         |          |                 |  |  |  |  |  |
| CO5        | Install and Configure FOSS server to provide different services                                 |         |         |          |                 |  |  |  |  |  |

# **CO-PO Mapping:**

| CO  | PO<br>1 | PO<br>2 | PO3 | PO4 | PO5 | PO6 | <b>PO7</b> | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
|-----|---------|---------|-----|-----|-----|-----|------------|-----|-----|------|------|------|------|------|
| CO1 | 2       |         |     |     |     |     |            | 1   | 2   | 2    |      | 1    |      | 2    |
| CO2 |         |         | 3   |     |     |     |            | 1   |     |      |      |      |      |      |
| CO3 |         | 1       |     |     | 2   |     |            | 1   |     |      |      |      | 2    |      |
| CO4 |         |         | 3   |     | 2   |     |            | 1   |     |      |      | 1    | 2    |      |
| CO5 |         |         |     |     | 2   | 1   | 1          | 1   |     |      |      |      |      |      |

Assessments :

Teacher Assessment:

One component of In Semester Evaluation (ISE) and one End Semester Examination (ESE) having 50% and 50% weights respectively.

|   | Marks   | Assessment  |         |  |  |  |  |  |  |
|---|---|---|---------|--|--|--|--|--|--|
|   | 25  | ISE   |         |  |  |  |  |  |  |
|   | 25 ESE(OE)  |   |         |  |  |  |  |  |  |
|   | LI  |   |         |  |  |  |  |  |  |
| Course C  | Contents:   |   |         |  |  |  |  |  |  |
| Experime  | ent No. 0:- Socket Programming API in C/C++   |   | 2 Hrs   |  |  |  |  |  |  |
| Experime  | ent No. 1:- Well Known Server and Client  |   | 2 Hrs   |  |  |  |  |  |  |
| Experime  | ent No. 2:- Routing Algorithm and Protocols   |   | 4 Hrs   |  |  |  |  |  |  |
| <ul> <li>A) In</li> <li>B) In</li> <li>C) S</li> </ul>                                | nplementation of Shortest Path routing algorithm in<br>nplementation of Distance Vector routing algorithm<br>imulation of Routing Protocols | n C/C++ programming language $m in C/C++$ programming language. |         |  |  |  |  |  |  |
| Experime<br>Class of a  | ent No. 3:- Implementation of C program to find N<br>given input IPv4 Address.  | etwork ID, Host ID and the network                              | 2 Hrs   |  |  |  |  |  |  |
| Experime  | ent No. 4:- Implementation of Iterative Client / Se   | erver Model using TCP Sockets                                   |         |  |  |  |  |  |  |
| Experime  | ent No. 5:- Implementation of Concurrent Client /   | Server Model using TCP Sockets.                                 | 2 Hrs   |  |  |  |  |  |  |
| Experime  | ent No. 6:- Implementation of Client / Server Mod   | el using UDP sockets.   | 2 Hrs   |  |  |  |  |  |  |
| Experime  | ent No. 7:- Communication using IPv6  |   | 2 Hrs   |  |  |  |  |  |  |
| Experime  | ent No. 8:- Packet Capturing and Analysis   |   | 2 Hrs   |  |  |  |  |  |  |
| Experime  | Experiment No. 9:- Demonstration of working of DHCP, DNS, FTP, SSH, TELNET protocols  |   |         |  |  |  |  |  |  |
| Experiment No. 10 :- Install and Configure different types of services on FOSS Server |   |   |         |  |  |  |  |  |  |
| Textbook  | KS:   |   |         |  |  |  |  |  |  |
| 1. Compu  | tter Networks - A Top-down Approach, Andrew S   | . Tanenbaum, Fifth Edition, Pearson Ed                          | ucation |  |  |  |  |  |  |
| 2.TCP/IP  | Protocol Suite by B. A. Forouzan, TMGH Publicat   | tion  |         |  |  |  |  |  |  |
| 3. Unix N   | letwork Programming – W. Rhichard Stevens Seco  | nd Edition (PHI)  |         |  |  |  |  |  |  |

4. Linux User guide available on Internet (freeware).

| Title of the  | Course: I             | Mini Pr       | oject     |          |  |          |          |               |             | L        | Г Р      | C        | redit |
|---|-----------------------|---------------|-----------|----------|--|----------|----------|---------------|-------------|----------|----------|----------|-------|
| Course Cod  | e: UCSE               | 0451          |           |          |  |          |          |               |             |          | 2        | 1        |       |
| Course Pre-   | Course Pre-Requisite: |               |           |          |  |          |          |               |             |          |          |          |       |
| UBSH0208- Computer Programming  |                       |               |           |          |  |          |          |               |             |          |          |          |       |
| UBSH0238- Computer Programming Lab  |                       |               |           |          |  |          |          |               |             |          |          |          |       |
| UCSE0303-Data Structures  |                       |               |           |          |  |          |          |               |             |          |          |          |       |
| Course Dese   | Data Stri             | Imploy        | Lau       | on of N  | /ini Dr                                |          | ainaD    | nogrom        | mina C      | oncont   | a        |          |       |
| Course Dest   | ripuon:<br>etives 7   | <u>Impien</u> | nentati   | onte to  | ////////////////////////////////////// | oject u  | Ising PI | rogram        |             | oncept   | 5.       |          |       |
|   | lentify th            | e proble      | m defi    | nition   |  |          |          |               |             |          |          |          |       |
| 2  To f   | ollow the             | method        | s and t   | asks of  | Softw                                  | are eng  | ineerin  | σ             |             |          |          |          |       |
| 3. To u   | ilize the             | e technio     | iues, ski | ills and | moder                                  | n engin  | eering   | 5<br>tools ne | cessarv     | for buil | ding th  | e projec | t     |
| <b>4.</b> To e  | fectively             | demon         | strate a  | nd pres  | ent the                                | ideas,   | method   | ology a       | ind techi   | nology   | used for | the pro  | ject  |
| Course Lean   | ning Ou               | tcomes:       | :         | •        |  |          |          |               |             | 07       |          |          | 9     |
| CO Aft  | er the co             | mpletio       | n of th   | e cours  | se the st                              | tudent   | should   | l be abl      | e to        |          |          |          |       |
|   |                       |               |           |          |  |          |          |               |             |          |          |          |       |
| CO1 Def   | ine the p             | roblem s      | statemer  | nt of th | e softw                                | are pro  | ject.    |               |             |          |          |          |       |
| CO2 Org   | anize an              | effecti       | ve proj   | ject pla | an with                                | n clear  | and fi   | nite ob       | ojectives   | and d    | ocumer   | nt the   |       |
| syn   | opsis and             | project       | reports   | •        |  |          |          |               |             |          |          |          |       |
| CO3 Mo  | lel the va            | arious m      | odules    | of proj  | ect with                               | n the he | lp of D  | FDs , F       | lowchar     | ts etc.  |          |          |       |
| CO4 Dev   | elop the              | modules       | s of pro  | posed s  | ystem.                                 |          |          |               |             |          |          |          |       |
| CO5 Der   | nonstrate             | the test      | cases f   | or vali  | lation c                               | fnron    | and eve  | tom           |             |          |          |          |       |
|   | 1011511 ate           | the test      | Cases I   | or vand  |  | n prope  | JSEU Sys | stem.         |             |          |          |          |       |
| CORON   | •                     |               |           |          |  |          |          |               |             |          |          |          |       |
| CO-PO Ma  | oping:                |               | I         |          | 1                                      | r        | 1        | r             |             |          | PO1      |          |       |
| COs PO1   | PO2                   | PO3           | PO4       | PO5      | PO6                                    | PO7      | PO8      | PO9           | <b>PO10</b> | PO11     | 2        | P301     | P302  |
| CO1   | 3                     |               |           |          |  |          |          |               |             |          |          | -        | 2     |
| ~~~   | 5                     |               |           |          |  |          |          |               |             |          |          | 2        | 2     |
| CO2   | 2                     |               |           |          |  |          |          |               | 2           | 2        |          | -        | -     |
| CO3   |                       |               |           |          |  |          |          |               |             |          |          | 3        | 2     |
|   | _                     | 3             |           | 2        |  |          |          |               |             |          |          | 2        | 2     |
| CO4   |                       | 3             |           |          |  |          |          | 2             |             |          | 2        | 2        | 2     |
| CO5   |                       |               | 2         |          |  |          |          |               |             |          |          | 2        | -     |
|   | _                     |               | Z         |          |  |          |          |               |             |          |          |          |       |
| Assessments   | :<br>accmont:         |               |           |          |  |          |          |               |             |          |          |          |       |
| One compon  | ent of In             | Semeste       | r Evalu   | uation ( | ISE) an                                | id one F | and Ser  | nester I      | Tyamina     | tion (F  | SF) hav  | ing 25 a | nd 50 |
| Marks respectively  |                       |               |           |          |  |          |          |               |             |          |          |          |       |
| Marks Assessment  |                       |               |           |          |  |          |          |               |             |          |          |          |       |
|   |                       |               |           |          |  |          |          |               |             |          |          |          |       |
|   |                       |               |           | 25       |  |          |          | ISE           | r           |          |          |          |       |
|   |                       |               |           | 50       |  |          |          | ESE(P         | DE)         |          |          |          |       |
|   |                       |               |           |          |  |          |          |               | ,           |          |          |          |       |
| Assessments :         Teacher Assessment:         One component of In Semester Evaluation (ISE) and one End Semester Examination (ESE) having 25 and 50         Marks respectively.         Marks       Assessment         25       ISE         50       ESE(POE) |                       |               |           |          |  |          |          |               | nd 50       |          |          |          |       |

#### **Course Contents:**

The mini project should be undertaken preferably by a group of 3-4 students who will jointly work and implement the project. The group will select a project with the approval of the guide and submit the name of the project with a synopsis, of the proposed work, of not more than 02 to 03 pages. The mini project should consist of defining the problem, analyzing, designing the solution and implementing it using a suitable programming language or tool. A presentation and demonstration based on the above work is to be given by the group. The work will be jointly assessed by a panel of teachers of the department. A hard copy of project report of the work done is to be submitted along with the softcopy of the project during ESE.

| Sr.<br>No. | Parameter               | Unacceptable<br>(E)        | Marginal<br>(D)                              | Adequate-Good<br>(B+C)  | Excellent<br>(A)  |
|------------|-------------------------|----------------------------|--|---|---|
| 1          | Requirement<br>Analysis | Irrelevant                 | Partially                                    | Properly with few points left                                 | Requirement analysis<br>with all possible<br>strategies defined |
| 2          | Design                  | No<br>meaningful<br>Design | Incomplete<br>System<br>Design               | Presence of system<br>design but no Proper<br>Detailed Design | Presence of Correct<br>system Design and<br>Detailed Design     |
| 3          | Coding &<br>Testing     | Code will not<br>run       | Code Runs<br>Partially                       | Code runs with few errors or warnings                         | Code runs without<br>errors for defined test<br>cases           |
| 4          | Report(Content)         | Not proper                 | Relevant but<br>no references<br>and details | Content with<br>relevant data and<br>few spelling errors      | Good Content with no spelling errors                            |

#### **Rubrics for Evaluation**

| Title of the Course: Soft Skills | L | Т | Ρ | Credit |
|----------------------------------|---|---|---|--------|
| Course Code:UCSE0461             | - | • | 2 | -      |
| Course Pre-Requisite:            |   |   |   |        |

**Course Description:** Soft skills are a combination of people skills, social skills, communication skills, character traits, attitudes, career attributes, social intelligence and emotional intelligence quotients among others that enable people to navigate their environment, work well with others, perform well, and achieve their goals with complementing hard skills.

#### **Course Objectives:**

- 12. Explain the importance of soft skills in corporate life.
- 13. Develop written skills of students to write corporate letters/emails.
- 14. Develop communication skills required for corporate etiquettes and
- ethics. 15. Develop presentation skills required for professional life.

16. Develop the ability to work in team.

#### **Course Learning Outcomes:**

| CO         | After the completion of the course the student should be           | Bloo  | 's Cognitive  |
|------------|--|-------|---------------|
|            | able to  | level | Descriptor    |
| CO1        | Make use of effective communication skills in the corporate world. | 3     | Applying      |
| CO2        | Construct effective business letters/emails.                       | 6     | Creating      |
| CO3        | Demonstrate the corporate etiquettes and ethics                    | 2     | Understanding |
| <b>CO4</b> | Construct effective business presentations.                        | 6     | Creating      |
| <b>CO5</b> | Work in team and show leadership skills.                           | 2     | Understanding |

#### **CO-PO Mapping:**

| CO      | PO<br>1 | PO<br>2 | <b>PO</b><br>3 | PO<br>4 | <b>PO</b><br>5 | PO<br>6 | <b>PO</b><br>7 | PO<br>8 | PO<br>9 | PO1<br>0 | PO1<br>1 | PO1<br>2 | PS<br>O 1 | PSO2 |
|---------|---------|---------|----------------|---------|----------------|---------|----------------|---------|---------|----------|----------|----------|-----------|------|
| CO<br>1 |         |         |                |         |                |         |                |         |         |          |          | 1        | 1         |      |
| CO<br>2 |         |         |                |         |                |         |                |         |         |          |          | 1        | 1         |      |
| CO<br>3 |         |         |                |         |                |         |                | 2       |         |          |          |          | 2         |      |
| CO<br>4 |         |         |                |         |                |         |                |         |         |          |          | 1        | 1         |      |
| CO<br>5 |         |         |                |         |                |         |                |         | 2       |          |          |          | 1         |      |

#### **Assessments : Audit Course**

| Course Contents:   |         |
|--|---------|
| Unit 1: Art of communication   | 02 Hrs. |
| Introduction to Soft Skills, Communication Theory, Effective Communication Skills, |         |
| Barriers and Filters, Active Listening, Non Verbal Communication, Body Language.   |         |
| Unit 2: Business Writing Skills  | 03 Hrs. |

| Business Letters/Emails - Format and Style, Types of Business Letter/Email – sales, order, complaint, adjustment, inquiry, follow-up, letter of recommendation, acknowledgement and resignation.  |         |
|---|---------|
| <b>Unit 3: World of teams</b><br>Team concept, Elements of team work, Building an effective team, Role of Team<br>Leader, Team based activities.  | 02 Hrs. |
| Unit 4: Adapting to corporate life  | 02 Hrs. |
| Corporate Grooming and dressing Business Etiquette Business Ethics Dinning Etiquette Ethics policy.   |         |
| Unit 5: Discussions, decisions and presentations<br>What are group discussions, Types of Group Discussions, Corporate Presentations,<br>Decision making, Resume Writing.  | 03 Hrs. |
| Unit 6: Job Interview: Types of Interviews -Telephonic, face to face, video, structured,  | 02 Hrs. |
| unstructured, behavioral, problem solving, panel, Importance of body language.  |         |
| <ul> <li>Textbooks:</li> <li>6. Personality Development and Soft- Skills, Barun K. Mitra, Oxford University Press.</li> <li>7. Business Communication : Making Connections in a Digital World 11th Edition<br/>(English, Paperback, Marie E. Flatley, Neerja Pande, Raymond V. Lesikar, Kathryn Rentz)</li> </ul> |         |
| Unit wise Measurable students Learning<br>Outcomes: Unit 1: Art of communication<br>UO1.1) To demonstrate the effective communication<br>skills. UO1.2) To make use of appropriate body<br>language.  |         |
| Unit 2: Business Writing Skills<br>UO2.1) To interpret the importance of business writing skills.<br>UO2.2) To apply the appropriate business etiquettes in business letter/email.  |         |
| <b>Unit 3: World of teams</b><br>UO3.1) To explain the importance of team in corporate<br>world. UO3.2) To demonstrate various team activities.   |         |
| Unit 4: Adapting to corporate life<br>UO4.1) To demonstrate business etiquettes and<br>ethics. UO4.2) To demonstrate corporate<br>dressing.   |         |
| Unit 5: Discussions, decisions and<br>presentations UO5.1) To demonstrate group<br>discussion activity. UO5.2) To apply<br>presentation skills in a presentation.   |         |